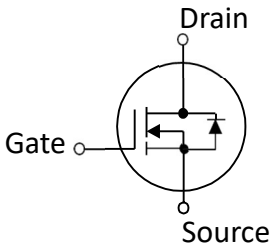
## *40V, 150A (1) N-Channel MOSFET*

- Proprietary Trench Gate Device Design and Processes
- High Reliability Capability
- Sampled CP Probing and Inking

**SYMBOL**



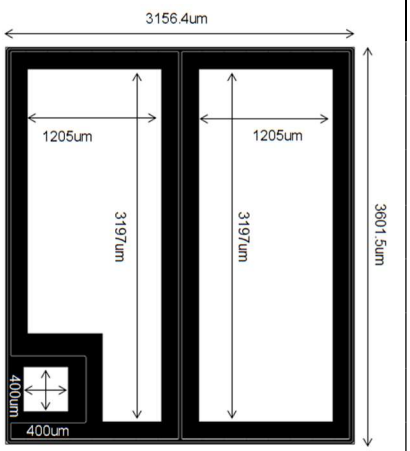

## Electrical Characteristics in C/P Test ($T_J$ at 25 ℃)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | 40 | — | — | V | $V_{GS}$ =0V, $I_D$ =250μA |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | — | 0.5 | 0.74 | mΩ | $V_{GS}$ =10V, $I_D$ =1A(2) |
| $V_{GS\ (th)}$ | Gate Threshold Voltage | 1.0 | — | 2.5 | V | $V_{DS}$ =$V_{GS}$, $I_D$ =250μA |
| $I_{DSS}$ | Drain-to-Source Leakage Current | — | — | 1 | μA | $V_{DS}$ =32V, $V_{GS}$ =0V |
| $I_{GSS}$ | Gate-to-Source Leakage Current | -100 | — | 100 | nA | $V_{DS}$ =0V, $V_{GS}$ =±20V |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature | -55℃ to 150℃ Max. | | | | |

## Mechanical Data

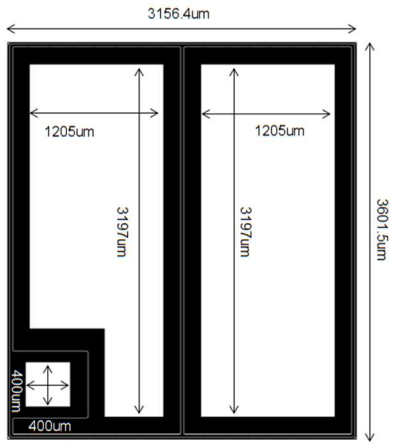
| | |
|---|---|
| Chip Size | 3156 μm X 3602 μm |
| Gate Pad Size | 400 μm X 400 μm |
| Source Pad Size 1 | 1205 μm X 3197 μm |
| Source Pad Size 2 | 1205 μm X 3197 μm |
| Scribe Line Width | 60 μm |
| Wafer Thickness | 150 μm |
| Wafer Diameter | 200 mm |
| Gross Die | 2385 EA |
| Source Metallization | Al-Cu (4μm typical) |
| Drain Metallization | Ti-Ni-Ag |
| Passivation | Yes |
| Recommended Storage Environment | Store in original container, in dry nitrogen, 6 months at ambient temperature of 23°C ± 3°C |

## Die Drawing



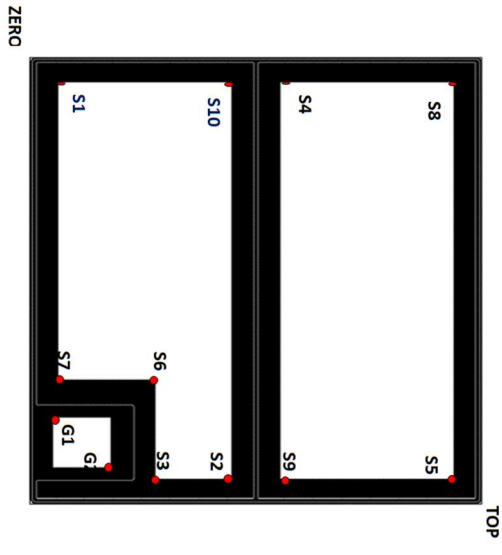

(1) This characteristic assumes the die is assembled in DFN5*6 package. Actual performance may degrade when assembled.

(2) Pulse Width tp = < 1 mS, Duty Cycle < 2%.

| Specific Assembly Information Bill of Material (BOM) | | Die Drawing |
|---|---|---|
| Package Type | DFN5*6 |  |
| Die Attach Method | Soft solder | |
| Soft Solder Composition | Pb,Sn,Ag | |
| Gate Wire Bonding | Cu, 2 mil x1 | |
| Source Wire Bonding | 60mil*4mil Al Ribbon (double stitch) | |
| Molding Compound Manufacturer | G700HF | |
| Solder Plating Composition | Pure Tin | |



| Position | | | Bonding Diagram Top View |
|---|---|---|---|
| | X (um) | Y (um) | |
| ZERO | 0 | 0 | |
| TOP | 3601.55 | 3156.4 | |
| S1 | 202.8 | 198.2 | |
| S2 | 3400 | 1403.5 | |
| S3 | 3400 | 878.2 | |
| S4 | 202.8 | 1752.9 | |
| S5 | 3400 | 2958.2 | |
| S6 | 2600 | 878.2 | |
| S7 | 2600 | 198.2 | |
| S8 | 202.8 | 2958.2 | |
| S9 | 3400 | 1752.9 | |
| S10 | 202.8 | 1403.5 | |
| G1 | 2907.92 | 160 | |
| G2 | 3307.92 | 560 | |



## Electrical Characteristics in F/P Test ($T_J$ at 25 ℃)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $I_{DSS}$ | Drain-to-Source Leakage Current | — | — | 1 | μA | $V_{DS}$ =32V, $V_{GS}$ =0V |
| $I_{GSSF}$ | Gate-to-Source Leakage Current | — | — | 100 | nA | $V_{DS}$ =0V, $V_{GS}$ =+20V |
| $I_{GSSR}$ | Gate-to-Source Leakage Current | -100 | — | — | nA | $V_{DS}$ =0V, $V_{GS}$ =-20V |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | 40 | — | — | V | $V_{GS}$ =0V, $I_D$ =250μA |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | 40 | — | — | V | $V_{GS}$ =0V, $I_D$ =1mA |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | — | — | 1.7 | mΩ | $V_{GS}$ =10V, $I_D$ =10A |
| $V_{GS\ (th)}$ | Gate Threshold Voltage | 1.0 | — | 2.5 | V | $V_{DS}$ =$V_{GS}$, $I_D$ =250μA |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | | | 1.1 | V | $V_{GS}$ = 0V, $I_{SD}$ = 10A |
| EAS test | IAS | | | | A | VDD=40V,Vgs=10V, RG=25ohm,L=0.5mH |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature | -55℃ to 150℃ Max. | | | | |

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