Description

40V N-CHANNEL ENHANCEMENT MODE POWER MOSFET

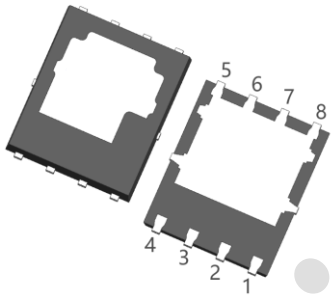
Features

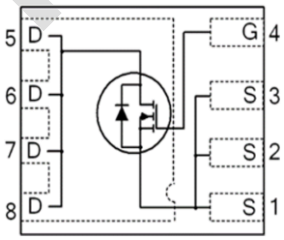
- Device Rating V_{DS} = 40V, I_D = 568A
- $R_{DS(ON)}$ =0.51mΩ (typ.) @ V_{GS} = 10V, I_D = 50A
- Proprietary High Density Trench Technology
- RoHS Compliant & Halogen-Free

Application

- High performance DC/DC
- SR
- Motor Driving

Package





DFN 5*6-8L Dual Cool

JFG568N40LC

Absolute Maximum Ratings T_C=25℃ unless otherwise specified

Symbol	Parameter		Max.	Units
V_{DS}	Drain-Source Voltage		40	V
V_{GS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current, VGS @ 10V note1	T_C = 25℃	568	A
		T_C = 100℃	359	A
I_{DM}	Pulsed Drain Current note2		1482	A
P_D	Power Dissipation note4	T_C = 25℃	312	W
	Power Dissipation	T_A = 25℃	2.5	W
E_{AS}	Single Pulsed Avalanche Energy note3		685	mJ
$R_{\theta JC}$	Thermal Resistance, Junction to Case bottom note1		0.4	℃/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case top note1		0.36	℃/W
$R_{\theta JA}$	Junction to Ambient (mounted on 1 inch square PCB)		50	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

Electrical Characteristics T_C=25℃ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	40	-	-	V
I_{DSS}	Drain-Source Leakage Current	V_{DS}=40V,V_{GS}= 0V, T_C = 25℃	-	-	1	μA
		V_{DS}=40V,V_{GS}= 0V, T_C = 55℃	-	-	10	μA
I_{GSS}	Gate-Source Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-100	-	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1.3	-	2.3	V
$R_{DS(on)}$	Static Drain-Source On-Resistance note2	V_{GS} = 10V, I_D =50A	-	0.51	0.65	mΩ
$R_{DS(on)}$	Static Drain-Source On-Resistance note2	V_{GS} = 4.5V, I_D =50A	-	0.69	0.85	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 1V, I_D =50A	-	260	-	S
Dynamic Characteristics						
R_g	Gate Resistance		-	1.1	-	Ω
C_{iss}	Input Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz	-	7990	-	pF
C_{oss}	Output Capacitance		-	1952	-	pF
C_{rss}	Reverse Transfer Capacitance		-	80	-	pF
Q_g	Total Gate Charge	V_{DS}=20V,I_D=50A,V_{GS} = 4.5V		56		nC
Q_g	Total Gate Charge	V_{DS} =20V, I_D = 50A, V_{GS} = 10V	-	118	-	nC
Q_{gs}	Gate-Source Charge		-	21	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	15	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 20V, I_D = 20A, R_G = 1Ω, V_{GS} = 10V	-	13	-	ns
t_r	Turn-On Rise Time		-	27	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	42	-	ns
t_f	Turn-Off Fall Time		-	15	-	ns
Source-Drain Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Diode Forward Current note1,5		-	-	260	A
I_{SM}	Maximum Pulsed Diode Forward Current note2,5		-	-	1482	A
t_{rr}	Reverse Recovery Time	T_J = 25°C, I_S = 10A, V_{GS} = 0V di/dt = 400A/μs	-	62	-	ns
Q_{rr}	Reverse Recovery Charge		-	186	-	nC
V_{SD} note2	Source to Drain Diode Forward Voltage	T_J = 25°C, I_S = 50A, V_{GS} = 0V	-	0.77	-	V

Note :

1.The data tested by surface mounted on one $inch^2$ FR-4 board with 2OZ copper.

2.The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.

3.The EAS data shows Max. rating. The test condition is L=0.1mH, I_D= 126A.

4.The power dissipation is limited by 150℃ junction temperature.

5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Performance Characteristics

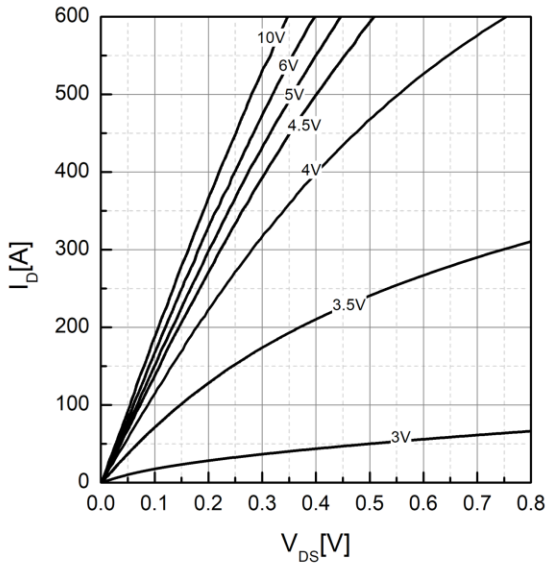


Figure 1. Output Characteristics, TJ=25℃

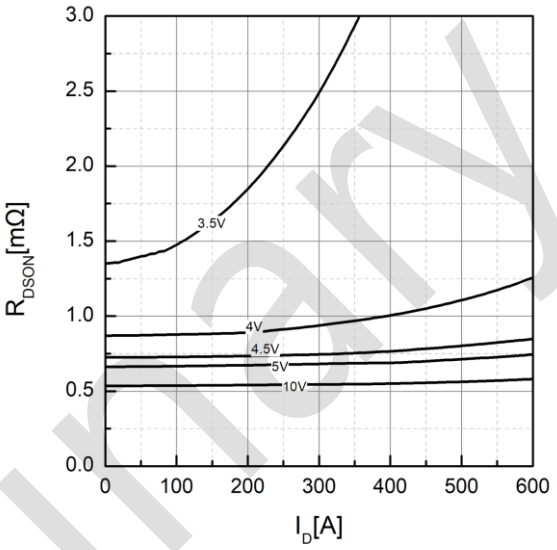


Figure 2. Drain-source on resistance , TJ=25℃

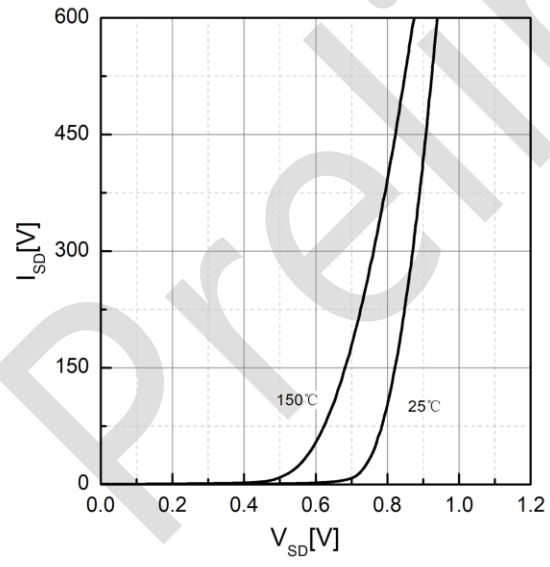


Figure 3. Forward characteristics of body diode

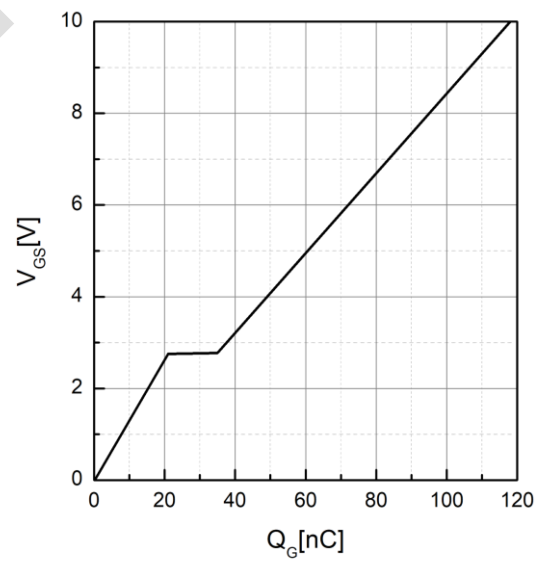


Figure 4. Gate Charge Characteristics

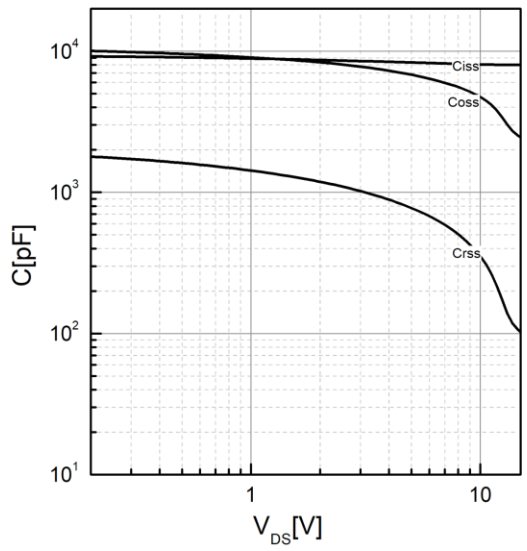


Figure 5. Capacitance Characteristics

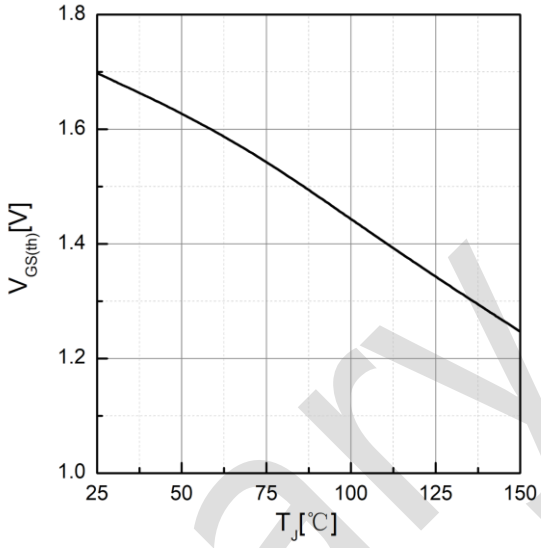


Figure 6. Threshold Voltage Vs. Temperature

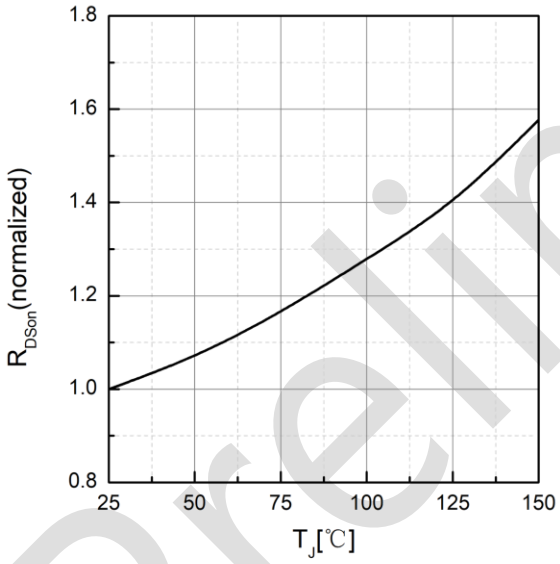


Figure 7. Drain-source on-state resistance

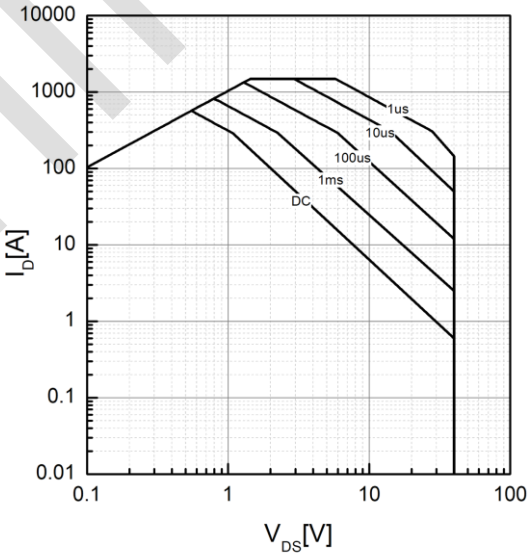


Figure 8. Maximum Safe Operating Area

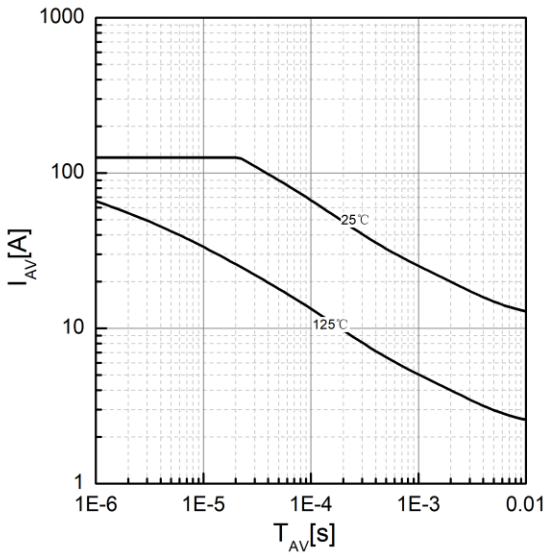


Figure 9. Avalanche characteristics

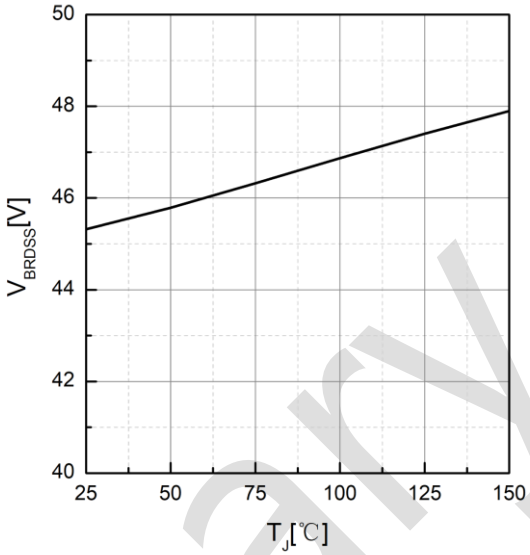


Figure 10. Drain-source breakdown voltage

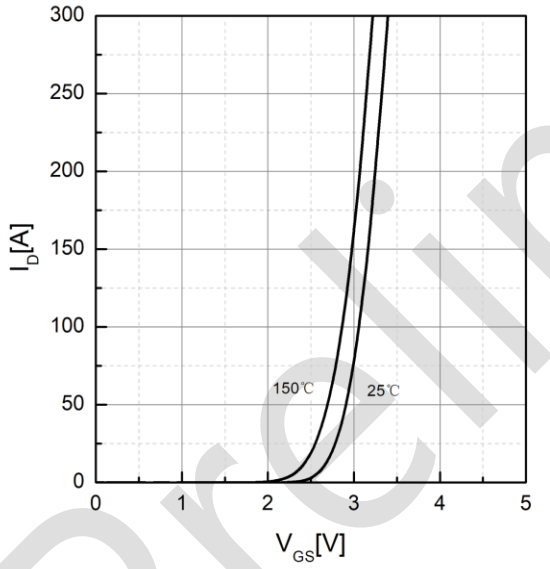


Figure 11. Transfer characteristics

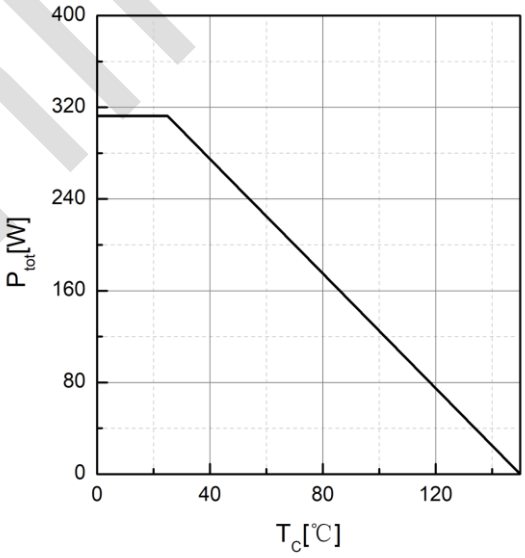


Figure 12. Power dissipation

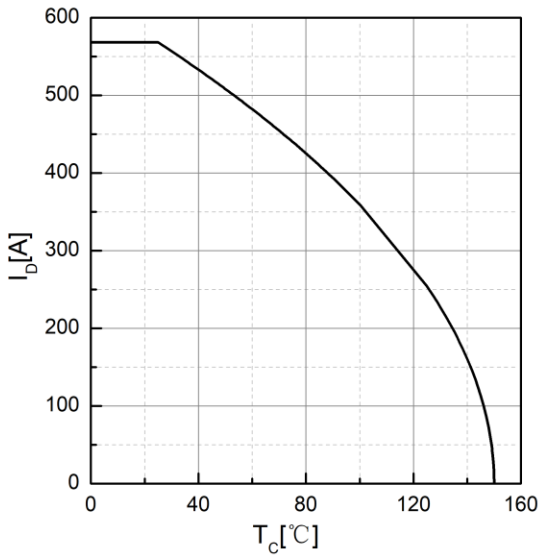


Figure 13. Drain current

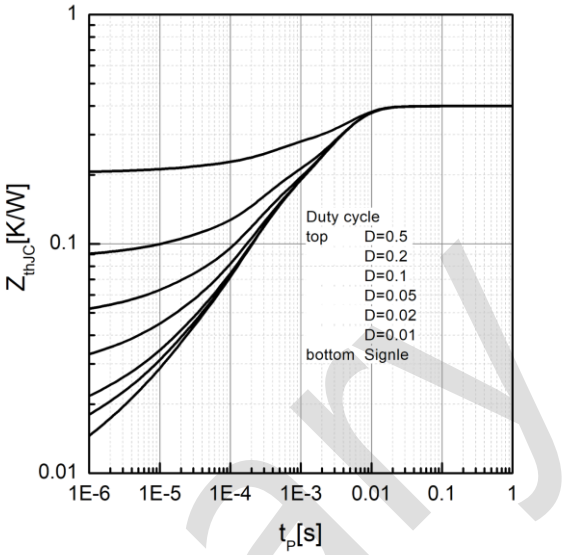


Figure 14. Effective Transient Thermal Impedance

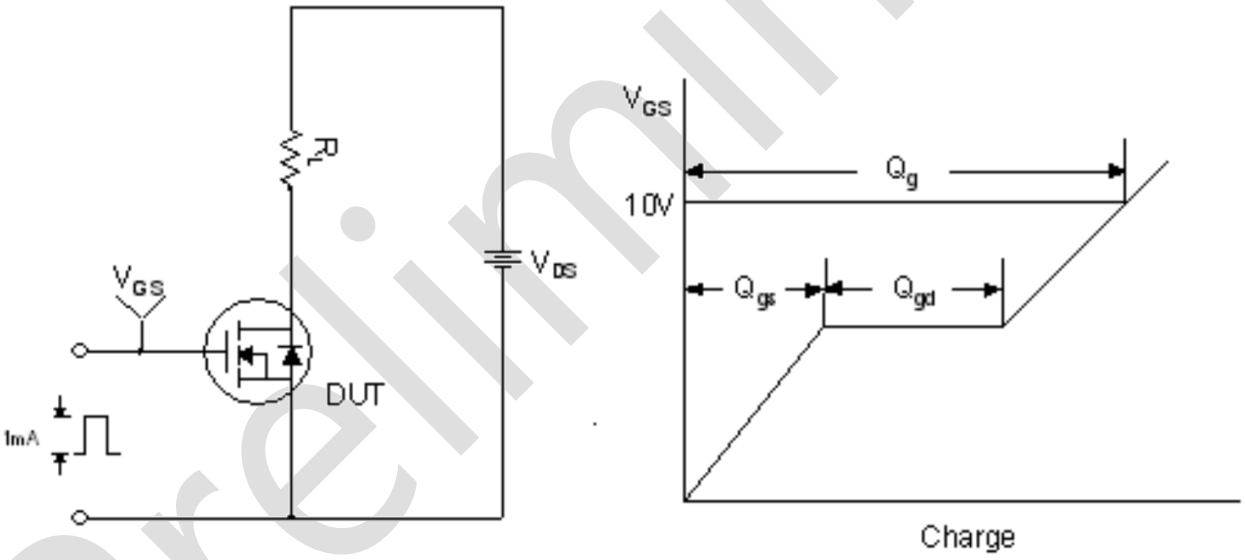


Figure 15. Gate Charge Test Circuit & Waveform

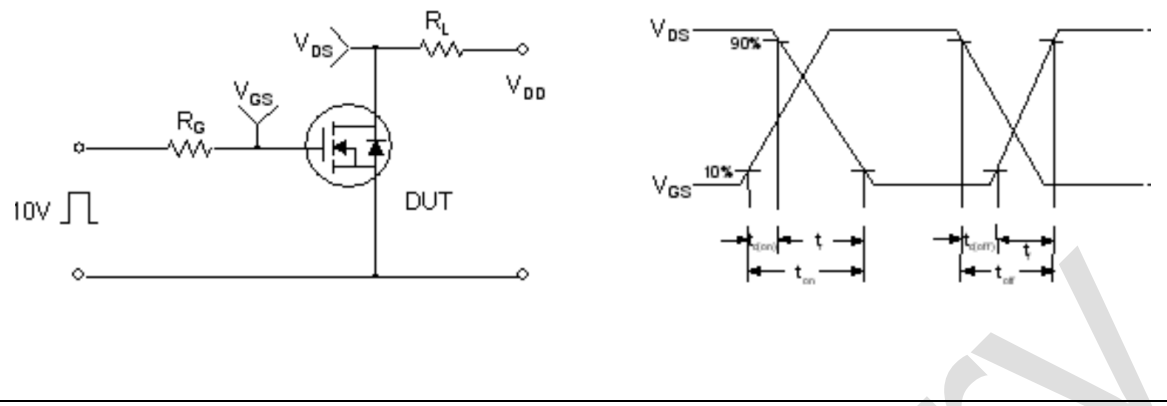


Figure 16. Resistive Switching Test Circuit & Waveforms

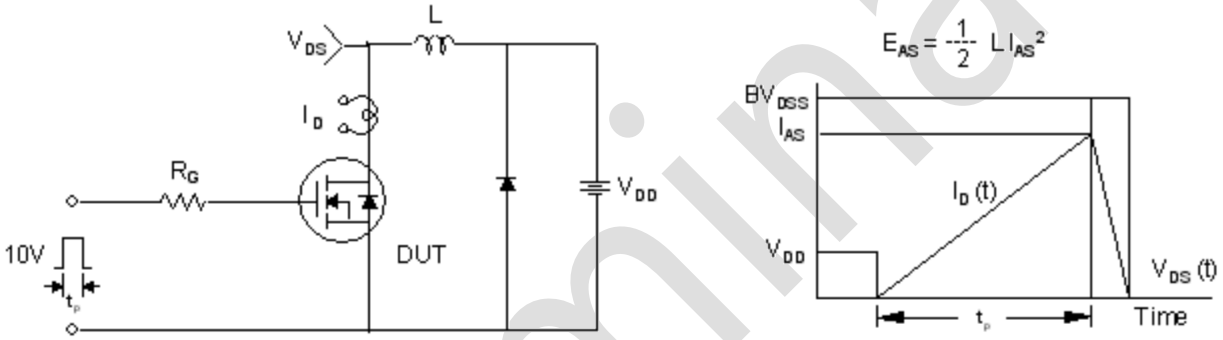


Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms

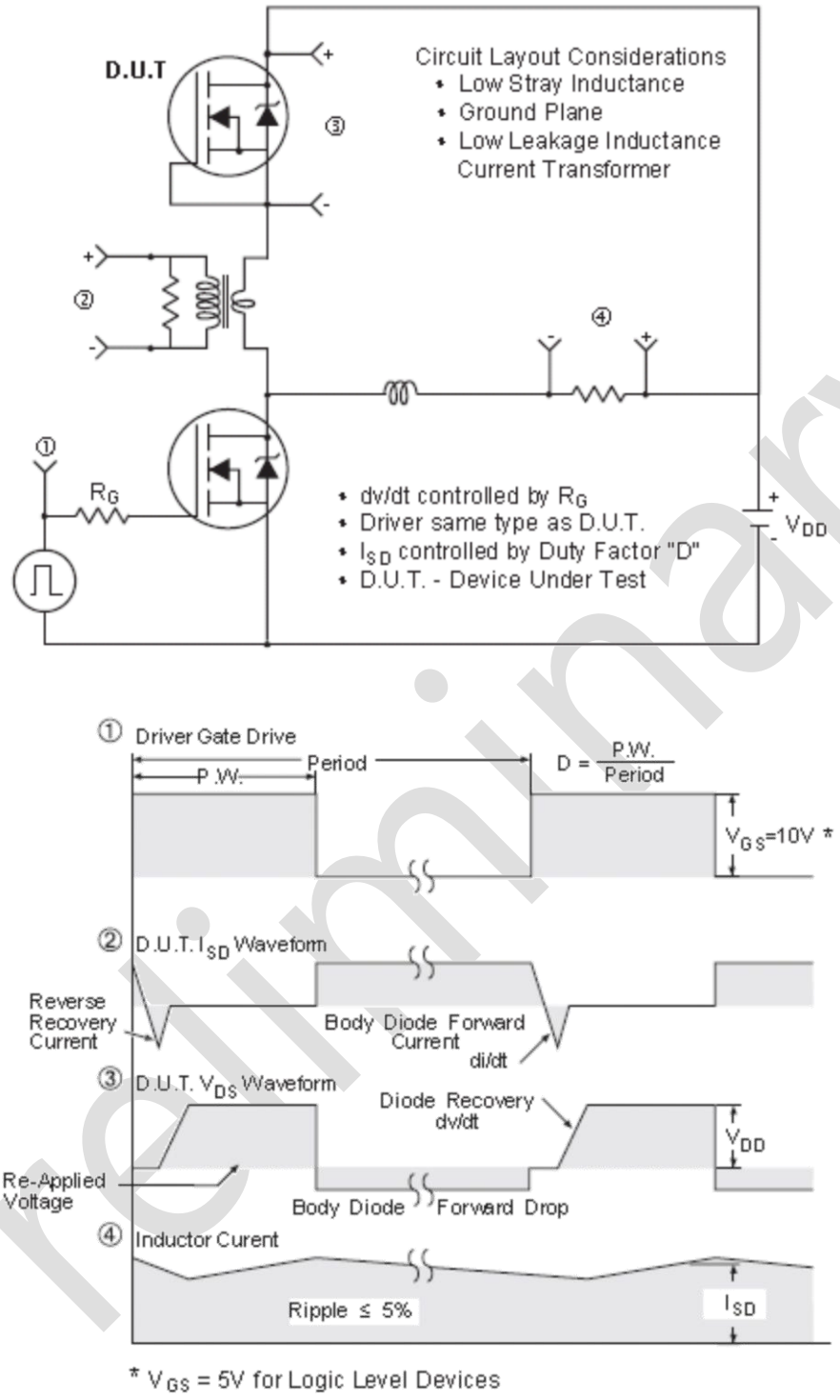
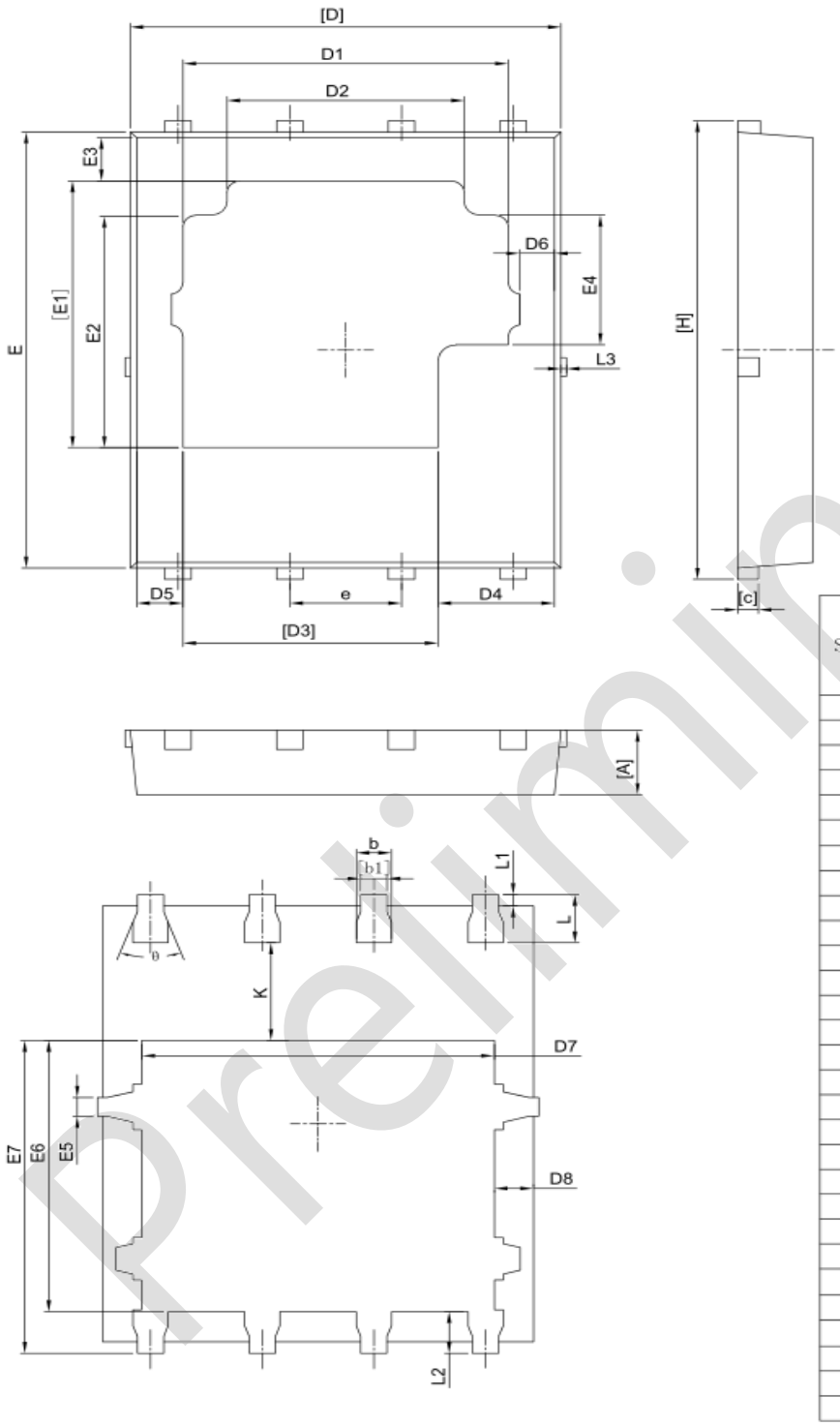


Figure 18. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

Package outline



SYMBOLS	DIMENSIONS MILLIMETERS		
	MIN	NOR	MAX
A	0.75	0.85	0.95
b	0.3	0.4	0.5
b1	0.2	0.3	0.4
c	0.2	0.25	0.3
D	4.8	5.0	5.2
D1	3.45	3.7	3.95
D2	2.45	2.7	2.95
D3	2.65	2.9	3.15
D4	1.08	1.33	1.58
D5	0.28	0.53	0.78
D6	0.2	0.4	0.6
D7	3.81	4.01	4.21
D8	0.24	0.44	0.64
E	5.55	5.75	5.95
E1	3.27	3.52	3.77
E2	2.80	3.05	3.30
E3	0.32	0.57	0.82
E4	1.46	1.71	1.96
E5	0.15	0.25	0.45
E6	3.32	3.57	3.82
E7	3.875	4.125	4.375
e	1.27bsc		
H	5.80	6.05	6.30
L	0.435	0.635	0.835
L1	0.05	0.15	0.25
L2	0.35	0.55	0.75
L3	–	0.06	0.85
K	1.09	1.29	1.49
θ	35°	40°	45°

Figure 19. DFN 5x6 Dual Cool Package outline

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