Description

40V N-CHANNEL ENHANCEMENT MODE POWER MOSFET

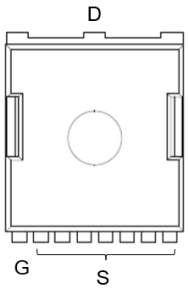
Features

- Device Rating V_{DS} = 40V, I_D = 537A
- $R_{DS(ON)}$ = 0.45mΩ (typ.) @ V_{GS} = 10V, I_D = 100A
- Advanced Split Gate Device Design
- RoHS Compliant & Halogen-Free
- Qualified according to JEDEC for target applications
- 100% avalanche test

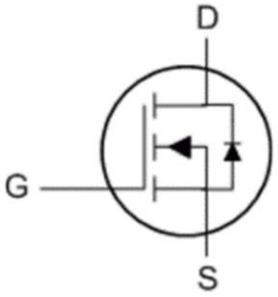
Application

- High frequency synchronous rectifiers
- Brushless DC motor control
- Battery protection
- High performance DC/DC converters
- OR-ing and redundant power switches

Package



TOLL
JFG537N40Q



Absolute Maximum Ratings T_C=25℃ unless otherwise specified

Symbol	Parameter		Max.	Units
V_{DS}	Drain-Source Voltage		40	V
V_{GS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current, VGS @ 10V note1	T_C = 25℃	537	A
		T_C = 100℃	340	A
I_{DM}	Pulsed Drain Current note2		TBD	A
P_D	Power Dissipation note4	T_C = 25℃	312	W
	Power Dissipation	T_A = 25℃	3.1	W
E_{AS}	Single Pulsed Avalanche Energy note3		TBD	mJ
$R_{\theta JC}$	Thermal Resistance, Junction to Case note1		0.4	℃/W
$R_{\theta JA}$	Junction to Ambient (mounted on 1 inch square PCB)		40	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

Electrical Characteristics T_C=25℃ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	40	-	-	V
I_{DSS}	Drain-Source Leakage Current	V_{DS} = 40V, V_{GS} = 0V, T_C = 25℃	-	-	1	μA
		V_{DS} = 40V, V_{GS} = 0V, T_C = 55℃	-	-	10	μA
I_{GSS}	Gate-Source Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-100	-	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1	-	2.4	V
$R_{DS(on)}$	Static Drain-Source On-Resistance note2	V_{GS} = 10V, I_D =100A	-	0.45	0.6	mΩ
		V_{GS} = 4.5V, I_D =50A	-	0.55	0.7	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10V, I_D =100A	-	TBD	-	S
Dynamic Characteristics						
R_g	Gate Resistance		-	TBD	-	Ω
C_{iss}	Input Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz	-	22000	-	pF
C_{oss}	Output Capacitance		-	4982	-	pF
C_{rss}	Reverse Transfer Capacitance		-	247	-	pF
Q_g	Total Gate Charge	V_{DS} =20V, I_D = 100A, V_{GS} = 4.5V	-	TBD	-	nC
Q_g	Total Gate Charge	V_{DS} =20V, I_D = 100A, V_{GS} = 10V	-	317	-	nC
Q_{gs}	Gate-Source Charge		-	64	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	46	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 20V, I_D = 30A, R_G = 1Ω, V_{GS} = 4.5V	-	TBD	-	ns
t_r	Turn-On Rise Time		-	TBD	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	TBD	-	ns
t_f	Turn-Off Fall Time		-	TBD	-	ns
Source-Drain Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Diode Forward Current note1,5		-	-	208	A
I_{SM}	Maximum Pulsed Diode Forward Current note2,5		-	-	TBD	A
t_{rr}	Reverse Recovery Time	T_J = 25°C, V_R = 34V, I_F = 100A, di/dt = 100A/μs	-	TBD	-	ns
Q_{rr}	Reverse Recovery Charge		-	TBD	-	nC
V_{SD} note2	Source to Drain Diode Forward Voltage	T_J = 25°C, I_S = 100A, V_{GS} = 0V	-	0.8	-	V

Note :

1.The data tested by surface mounted on one $inch^2$ FR-4 board with 2OZ copper.

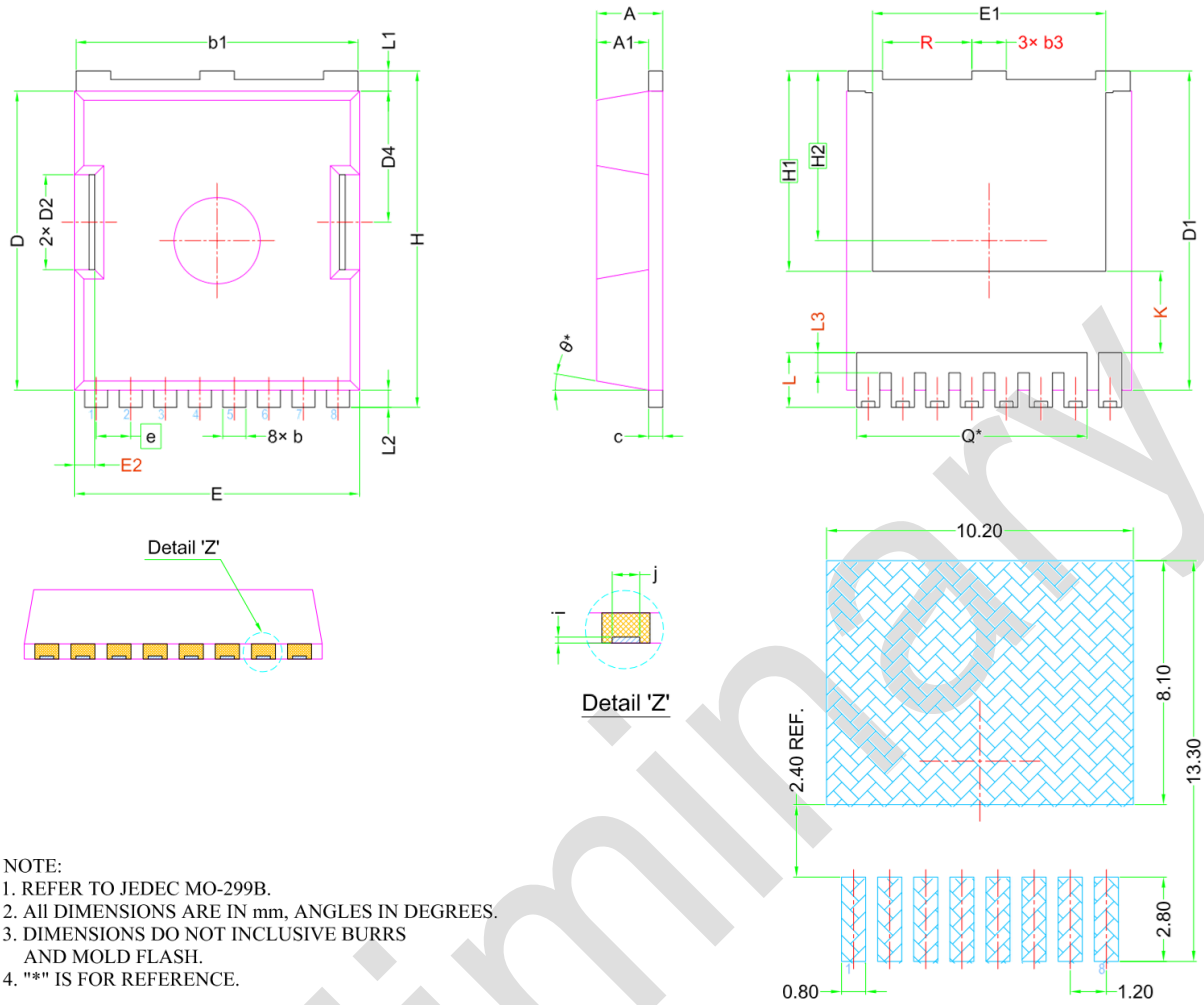
2.The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.

3.The EAS data shows Max. rating. The test condition is L=0.1mH, I_{AS}= TBD A.

4.The power dissipation is limited by 150°C junction temperature.

5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Package outline



NOTE:
1. REFER TO JEDEC MO-299B.
2. All DIMENSIONS ARE IN mm, ANGLES IN DEGREES.
3. DIMENSIONS DO NOT INCLUSIVE BURRS AND MOLD FLASH.
4. "*" IS FOR REFERENCE.

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b3	1.10	1.20	1.30
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D4	4.45	4.55	4.65
E	9.80	9.90	1 0.00
E1	8.00	8.10	8.20
E2	0.60	0.70	0.80
e	1.20 BSC		

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
H	11.58	11.68	11.78
H1	6.95 BSC		
H2	5.89 BSC		
i	0.10 REF.		
j	0.46 REF.		
K	2.80 REF.		
L	1.40	1.90	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.30	0.70	0.80
N	8		
Q	8.00 REF.		
R	3.00	3.10	3.20
θ	10° REF.		

Figure 19. TOLL Package outline

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