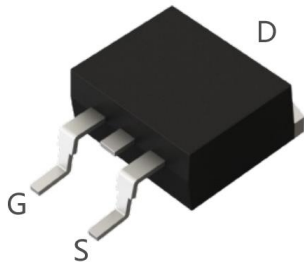


Description
40V N-CHANNEL ENHANCEMENT MODE POWER MOSFET
Features

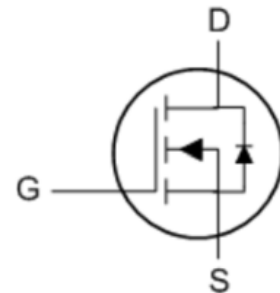
- Device Rating $V_{DS} = 40V$, $I_D = 311A$
- $R_{DS(ON)} = 1.0m\Omega$ (typ.) @ $V_{GS} = 10V$, $I_D = 20A$
- $R_{DS(ON)} = 1.4m\Omega$ (typ.) @ $V_{GS} = 4.5V$, $I_D = 20A$
- Proprietary High Density Trench Technology
- RoHS Compliant & Halogen-Free

Application

- BLDC
- BMS

Package


TO263-3L
JFG311N40E


Absolute Maximum Ratings $T_C=25^\circ C$ unless otherwise specified

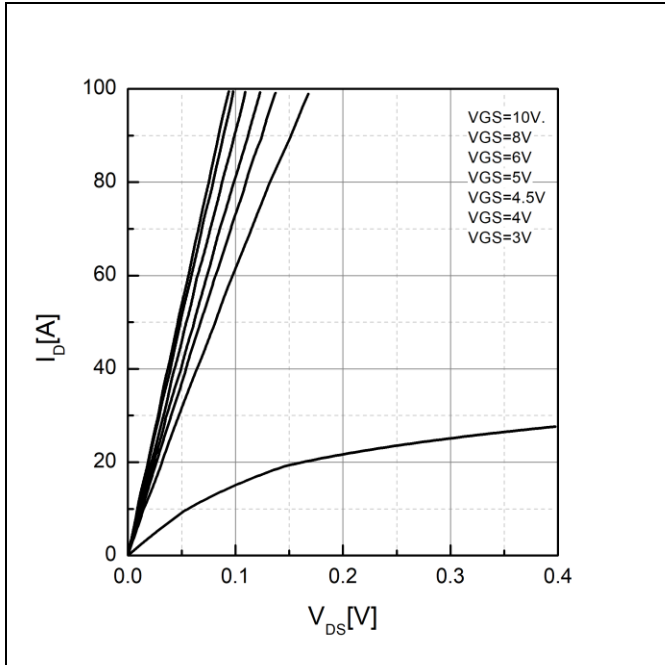
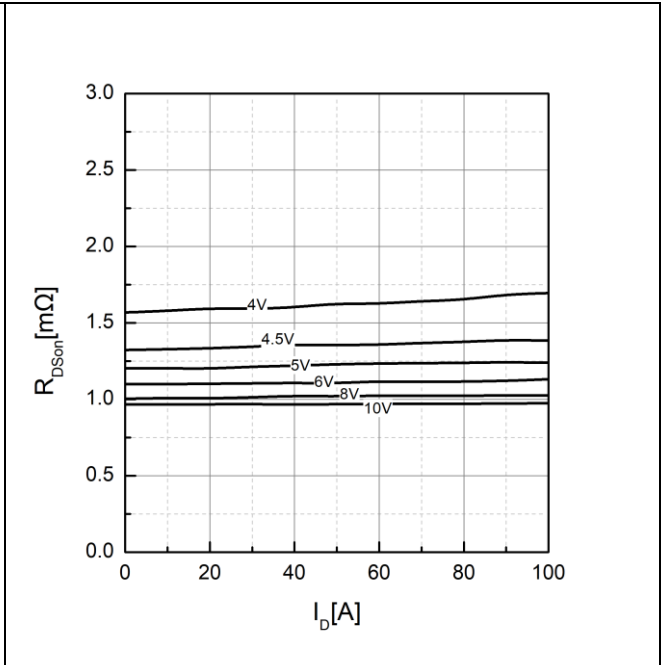
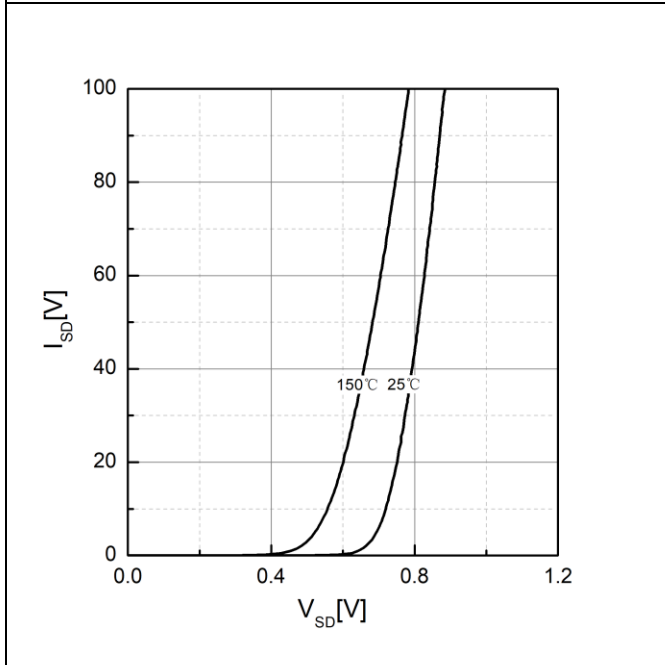
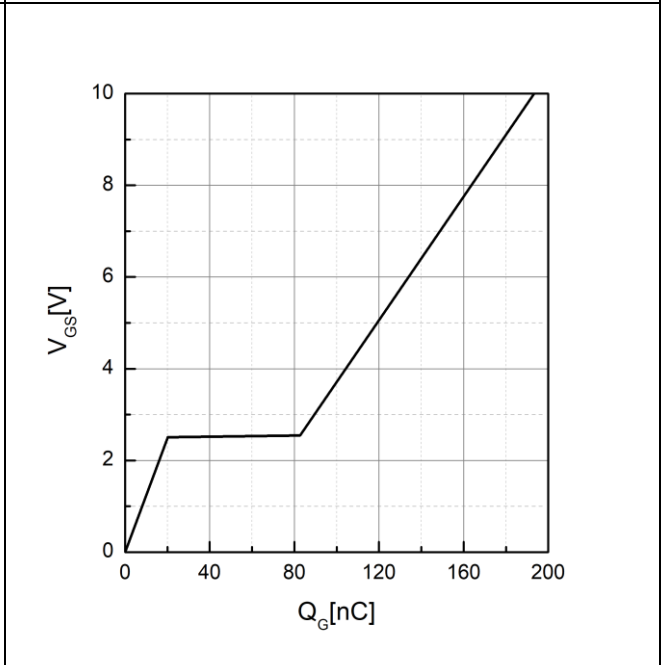
Symbol	Parameter	Max.	Units	
V_{DS}	Drain-Source Voltage	40	V	
V_{GS}	Gate-Source Voltage	± 20	V	
I_D	Continuous Drain Current, $V_{GS} @ 10V$ ^{note1}	$T_C = 25^\circ C$	311	A
		$T_C = 100^\circ C$	197	A
I_{DM}	Pulsed Drain Current ^{note2}	1250	A	
P_D	Power Dissipation ^{note4}	$T_C = 25^\circ C$	186	W
	Power Dissipation	$T_A = 25^\circ C$	8.8	W
E_{AS}	Single Pulsed Avalanche Energy ^{note3}	590	mJ	
$R_{\theta JC}$	Thermal Resistance, Junction to Case ^{note1}	0.67	$^\circ C/W$	
$R_{\theta JA}$	Junction to Ambient (mounted on 1 inch square PCB)	14.2	$^\circ C/W$	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$	

Electrical Characteristics $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	40	-	-	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS} = 40V, V_{GS} = 0V, T_C = 25^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 40V, V_{GS} = 0V, T_C = 55^\circ\text{C}$	-	-	10	μA
I_{GSS}	Gate-Source Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$	-100	-	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0	-	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance <small>note2</small>	$V_{GS} = 10V, I_D = 20A$	-	1.0	1.2	m Ω
		$V_{GS} = 4.5V, I_D = 20A$	-	1.4	1.7	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10V, I_D = 20A$		98	-	S
Dynamic Characteristics						
R_g	Gate Resistance		-	1.0	-	Ω
C_{iss}	Input Capacitance	$V_{DS} = 20V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$	-	8331	-	pF
C_{oss}	Output Capacitance		-	1378	-	pF
C_{rss}	Reverse Transfer Capacitance		-	1323	-	pF
Q_g	Total Gate Charge	$V_{DS} = 20V, I_D = 20A,$ $V_{GS} = 10V$	-	193	-	nC
Q_{gs}	Gate-Source Charge		-	20.2	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	62.5	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20V, I_D = 20A,$ $R_G = 1\Omega, V_{GS} = 10V$	-	52	-	ns
t_r	Turn-On Rise Time		-	108	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	100	-	ns
t_f	Turn-Off Fall Time		-	76	-	ns
Source-Drain Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Diode Forward Current <small>note1,5</small>		-	-	155	A
I_{SM}	Maximum Pulsed Diode Forward Current <small>note2,5</small>		-	-	1250	A
t_{rr}	Reverse Recovery Time	$T_J = 25^\circ\text{C}, I_S = 20A, V_{GS} = 0V$	-	48	-	ns
Q_{rr}	Reverse Recovery Charge	$T_J = 25^\circ\text{C}, I_S = 20A,$ $di/dt = 160A/\mu s$		74.5		nC
V_{SD} <small>note2</small>	Source to Drain Diode Forward Voltage	$T_J = 25^\circ\text{C}, I_S = 20A, V_{GS} = 0V$	-	0.72	-	V

Note :

- The data tested by surface mounted on one inch² FR-4 board with 2OZ copper.
- The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- The EAS data shows Max. rating. The test condition is $V_{DD}=40V, V_{GS}=10V, L=0.1mH, I_{AS}= 108 A$.
- The power dissipation is limited by 150°C junction temperature.
- The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Typical Performance Characteristics

Figure 1. Output Characteristics, $T_J = 25^\circ\text{C}$

Figure 2. Drain-source on resistance , $T_J = 25^\circ\text{C}$

Figure 3. Forward characteristics of body diode

Figure 4. Gate Charge Characteristics

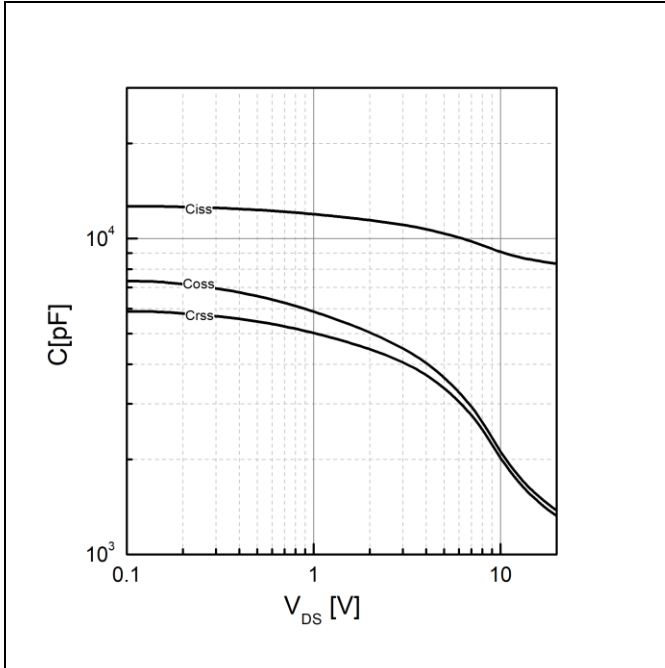


Figure 5. Capacitance Characteristics

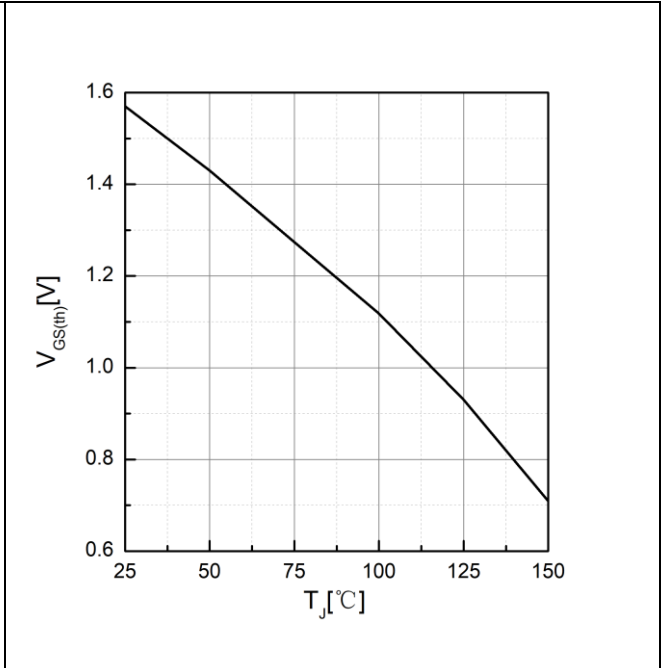


Figure 6. Threshold Voltage Vs. Temperature

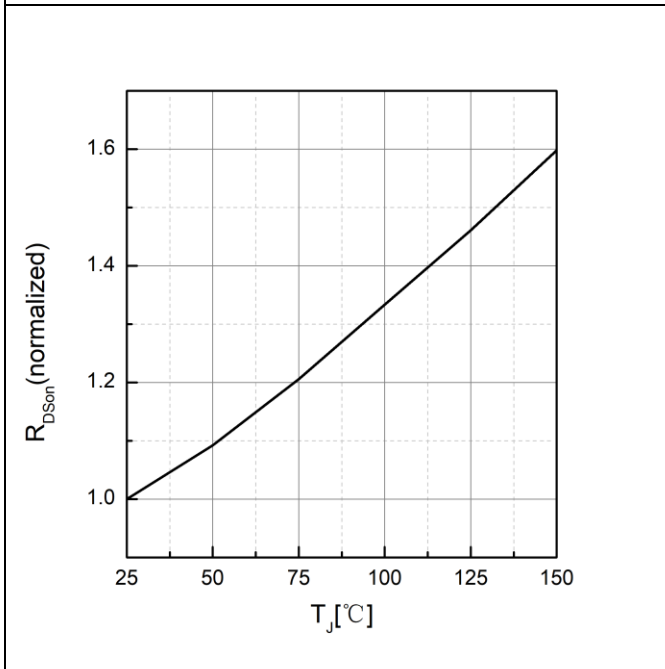


Figure 7. Drain-source on-state resistance

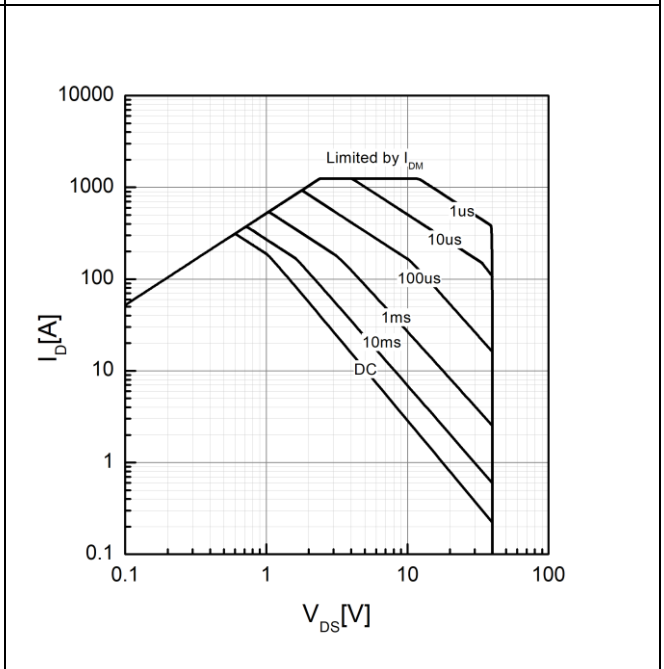


Figure 8. Maximum Safe Operating Area

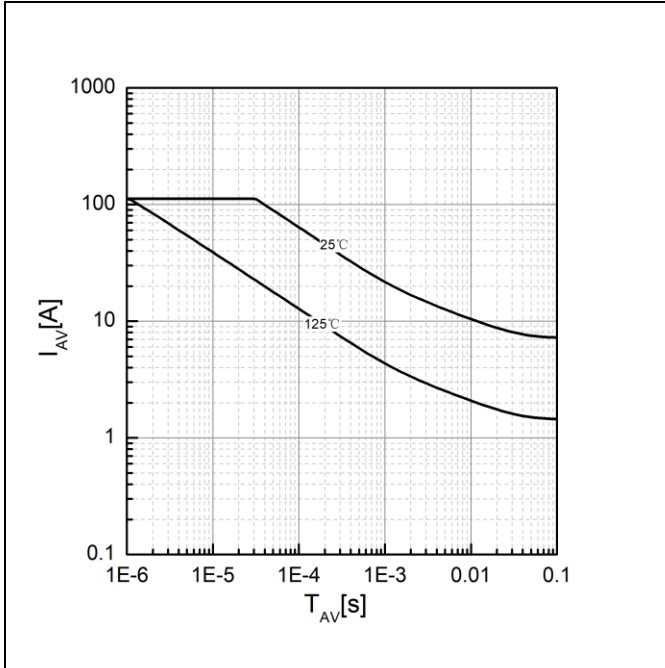


Figure 9. Avalanche characteristics

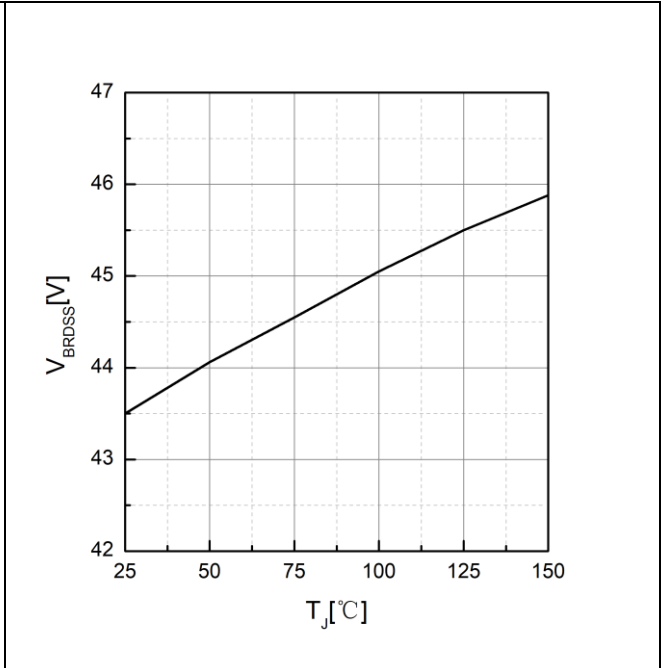


Figure 10. Drain-source breakdown voltage

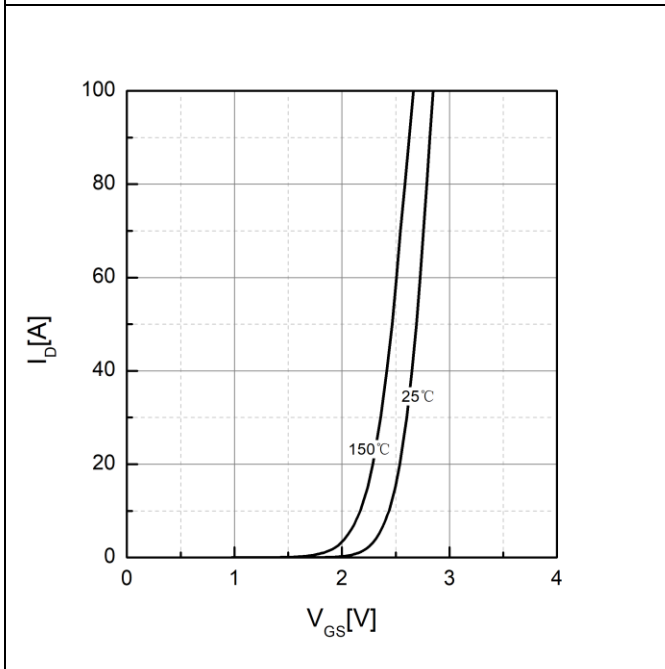


Figure 11. Transfer characteristics

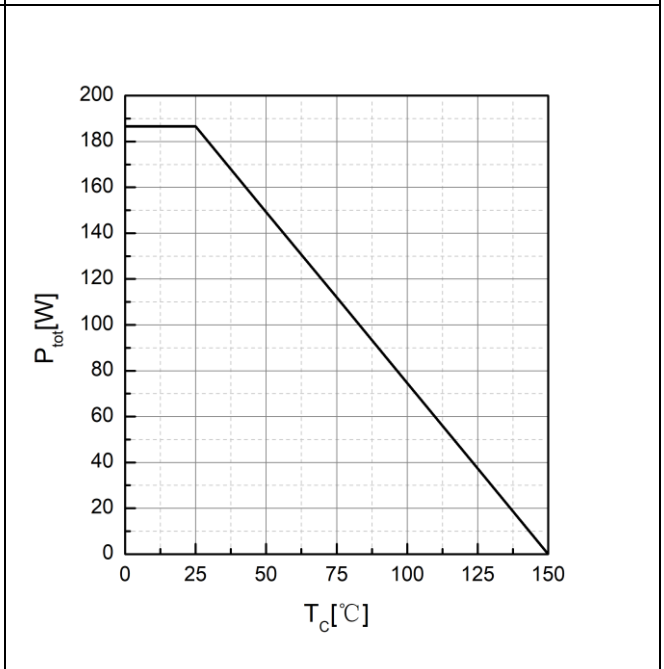


Figure 12. Power dissipation

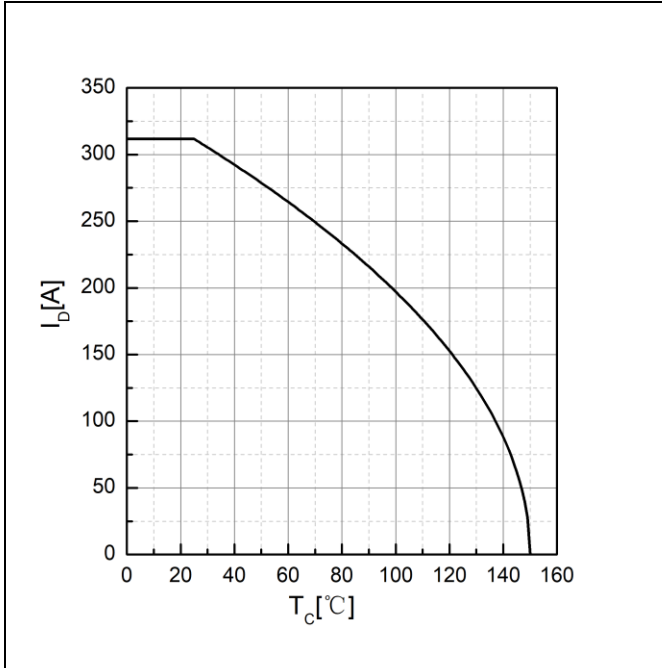


Figure 13. Drain current

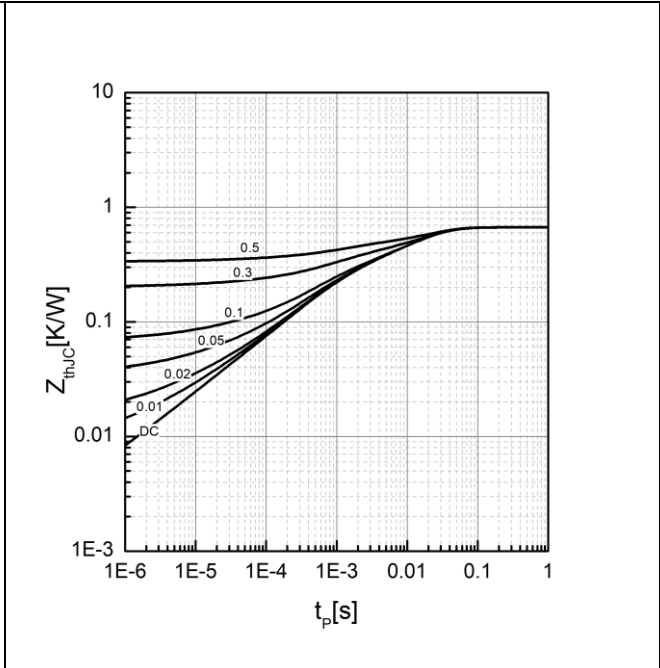


Figure 14. Effective Transient Thermal Impedance

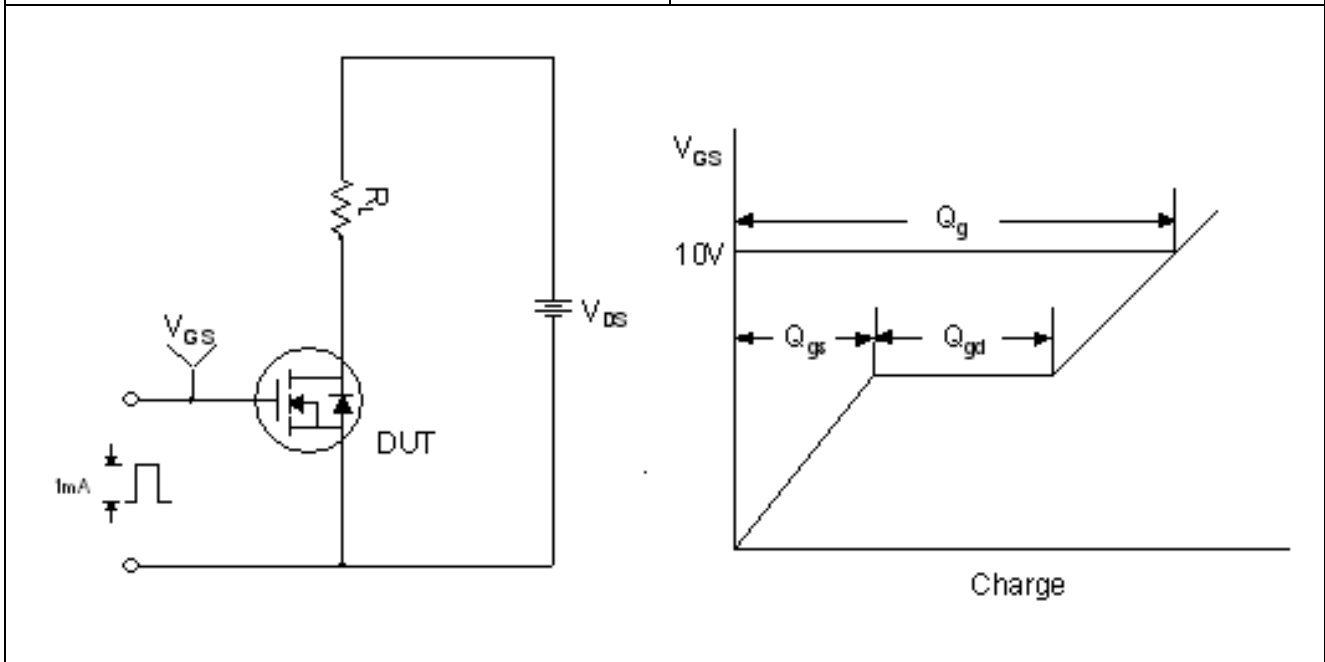


Figure 15. Gate Charge Test Circuit & Waveform

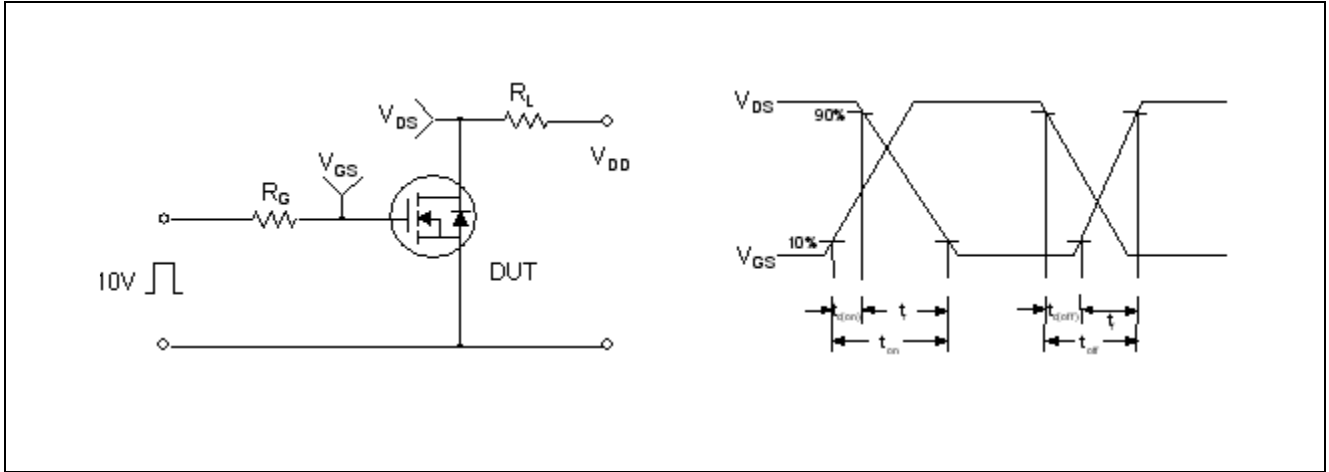


Figure 16. Resistive Switching Test Circuit & Waveforms

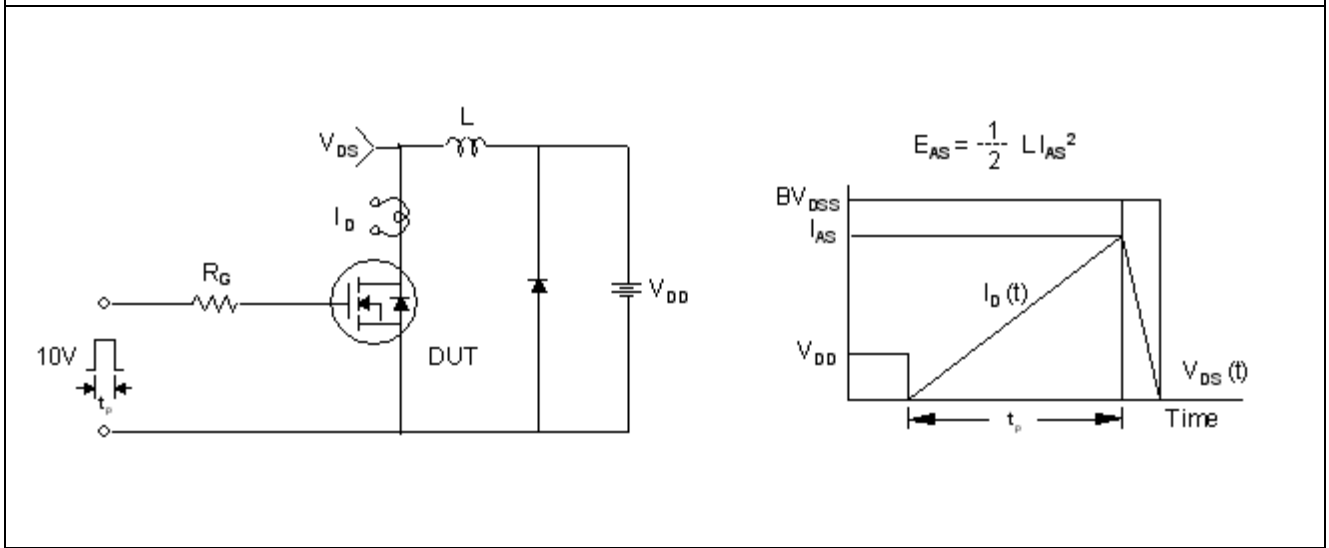


Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms

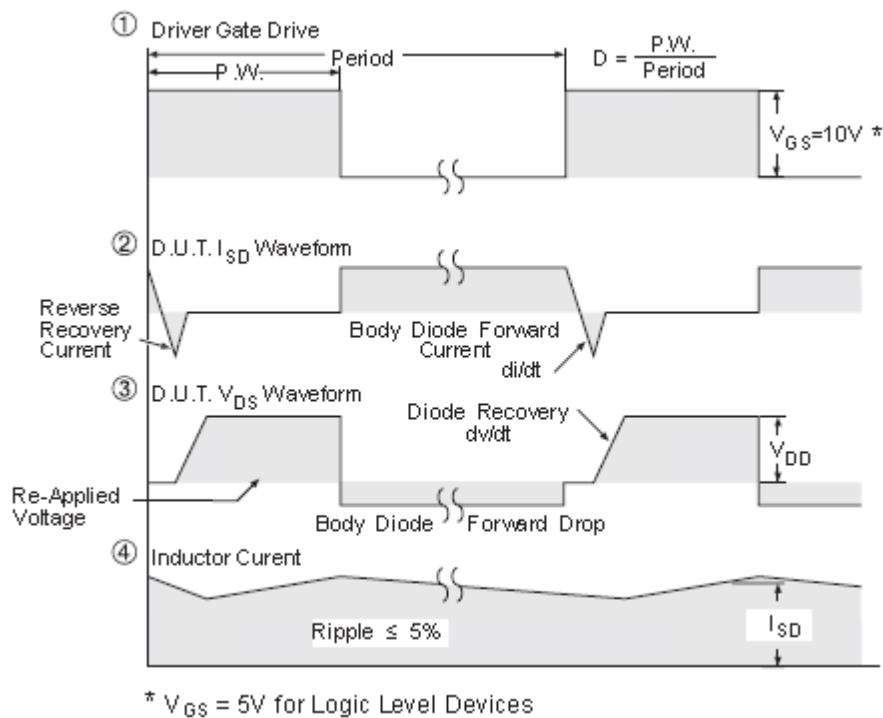
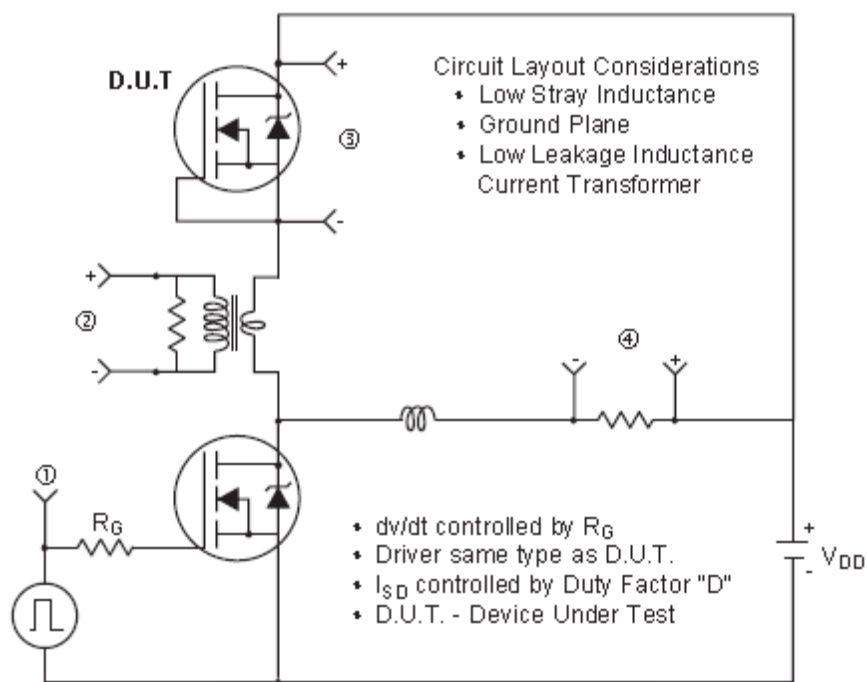
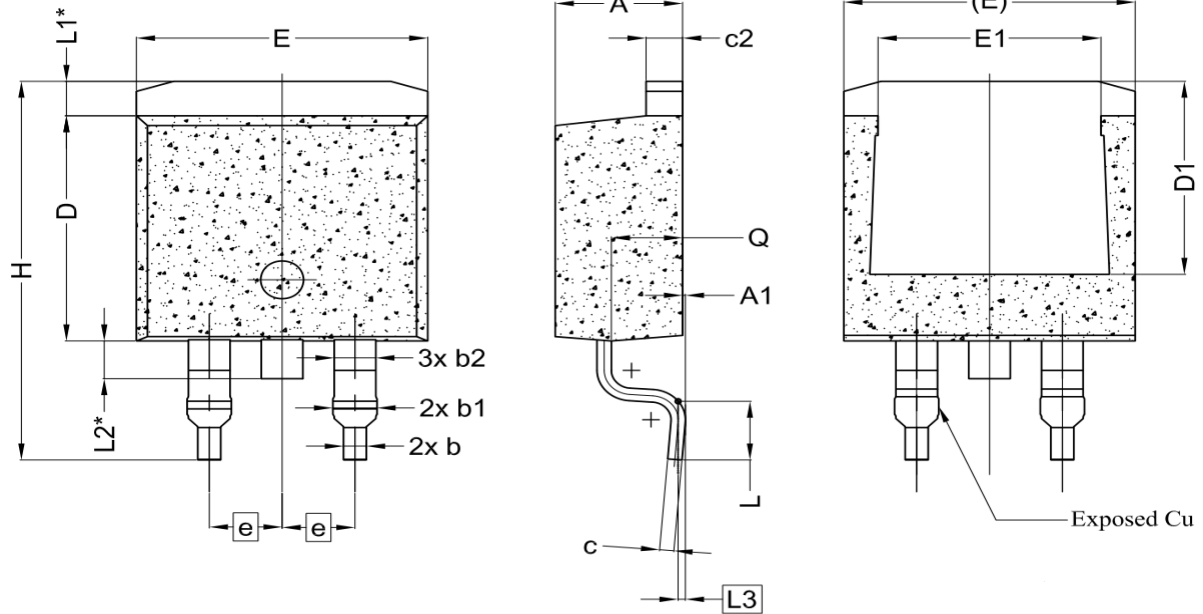
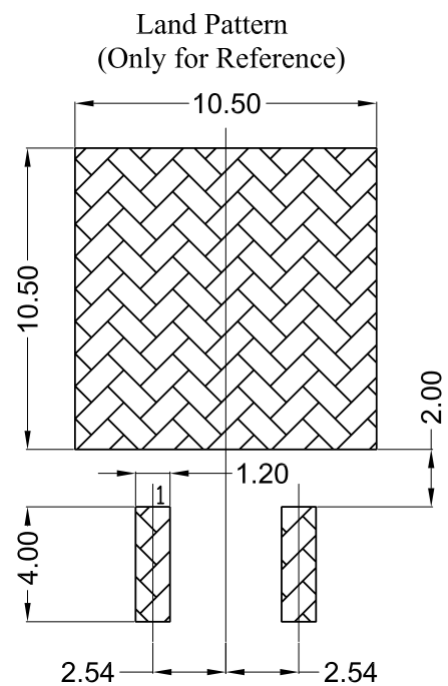


Figure 18. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

Package outline


SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	4.24	4.44	4.64
A1	0.00	0.10	0.25
b	0.70	0.80	0.90
b1	1.20	1.55	1.75
b2	1.20	1.45	1.70
c	0.40	0.50	0.60
c2	1.15	1.27	1.40
D	8.82	8.92	9.02
D1	6.86	7.65	---
E	9.96	10.16	10.36
E1	6.89	7.77	7.89
e	2.54 BSC		
H	14.61	15.00	15.88
L	1.78	2.32	2.79
L1	1.36 REF.		
L2	1.50 REF.		
L3	0.25 BSC		
Q	2.30	2.48	2.70


Figure 19. TO263-3L Package outline

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