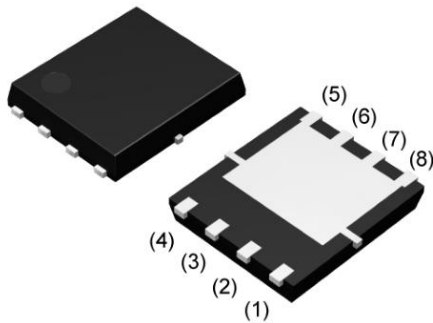


**Description**
**30V N-CHANNEL ENHANCEMENT MODE POWER MOSFET**
**Features**

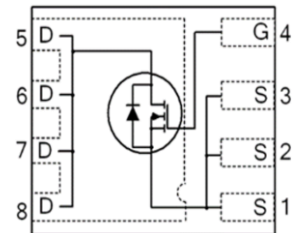
- Device Rating  $V_{DS} = 30V$ ,  $I_D = 265A$
- $R_{DS(ON)} = 1.4m\Omega$  (typ.) @  $V_{GS} = 10V$ ,  $I_D = 50A$
- Proprietary High Density Trench Technology
- RoHS Compliant & Halogen-Free

**Application**

- Battery Management System
- Load Switch
- Brushless DC Motor Control

**Package**


**DFN5\*6**  
**JFG265N30L**


**Absolute Maximum Ratings**  $T_C=25^\circ C$  unless otherwise specified

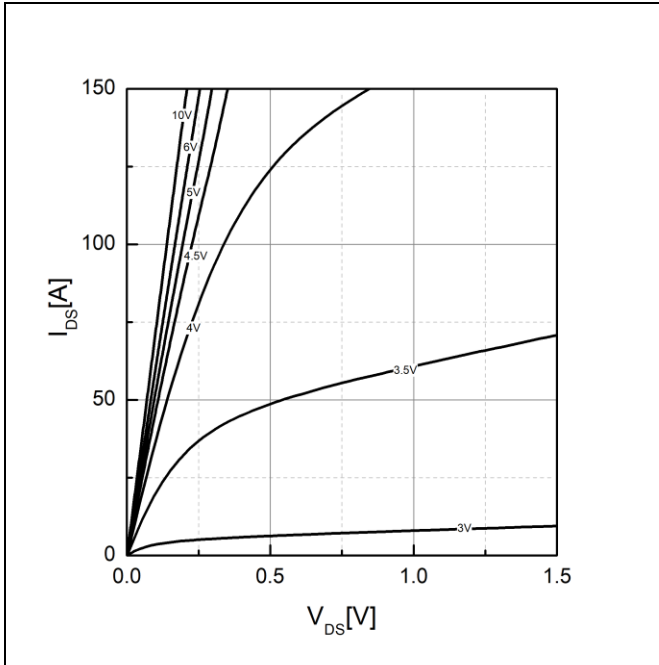
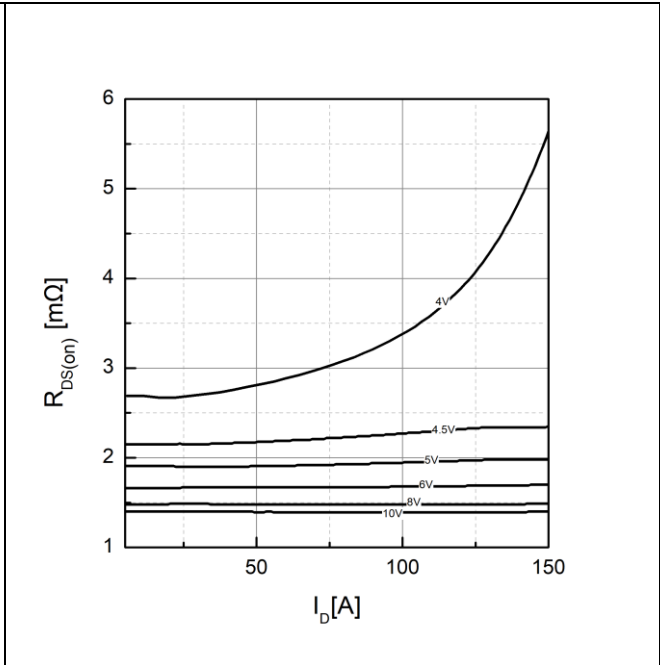
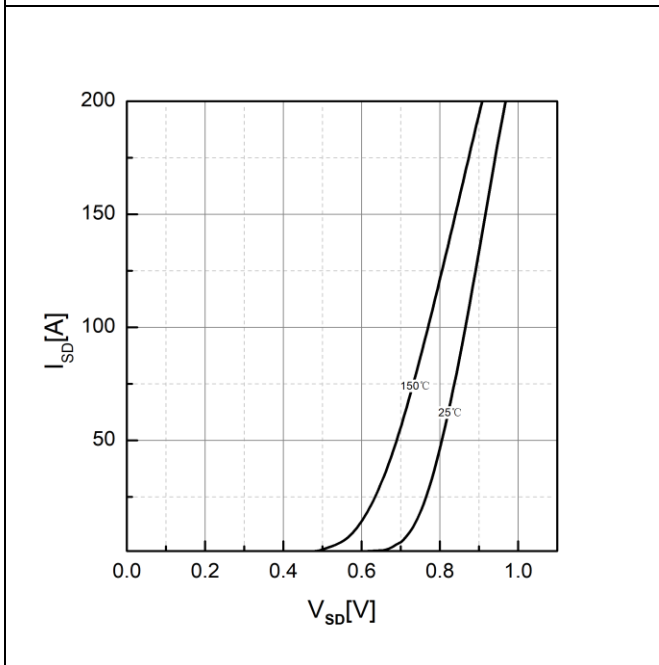
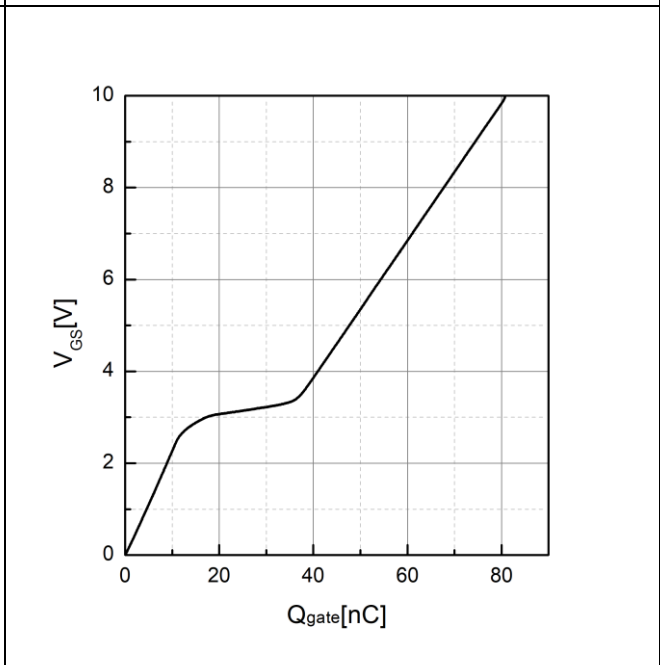
Symbol	Parameter	Max.	Units	
$V_{DS}$	Drain-Source Voltage	30	V	
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V	
$I_D$	Continuous Drain Current, $V_{GS} @ 10V$ <sup>note1</sup>	$T_C = 25^\circ C$	265	A
		$T_C = 100^\circ C$	168	A
$I_{DM}$	Pulsed Drain Current <sup>note2</sup>	1060	A	
$P_D$	Power Dissipation <sup>note4</sup>	$T_C = 25^\circ C$	136	W
	Power Dissipation	$T_A = 25^\circ C$	2.93	W
$E_{AS}$	Single Pulsed Avalanche Energy <sup>note3</sup>	454	mJ	
$R_{\theta JC}$	Thermal Resistance, Junction to Case <sup>note1</sup>	0.92	$^\circ C/W$	
$R_{\theta JA}$	Junction-to-Ambient (mounted on 1 inch square PCB)	42.6	$^\circ C/W$	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$	

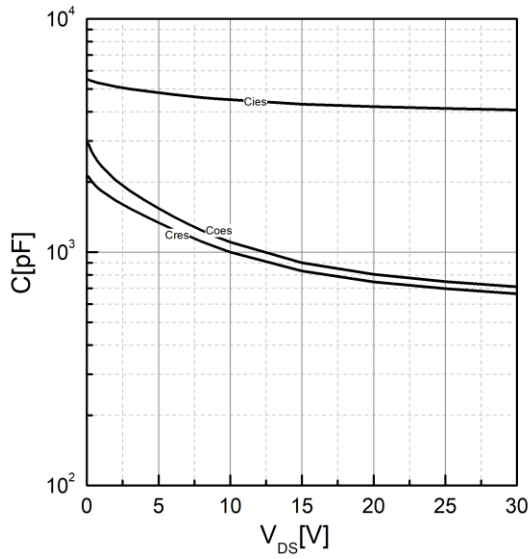
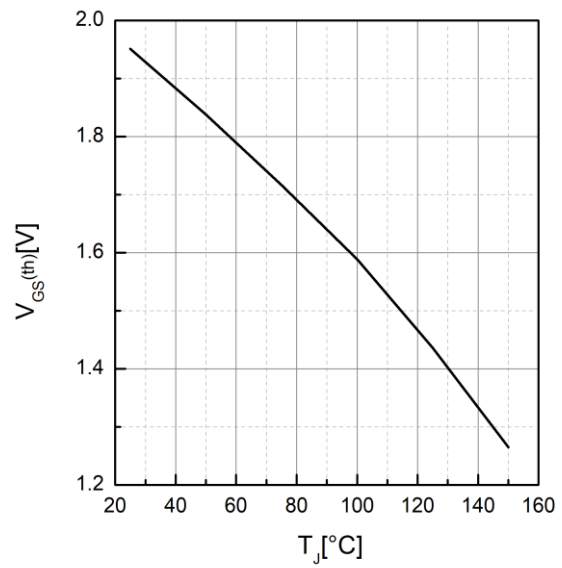
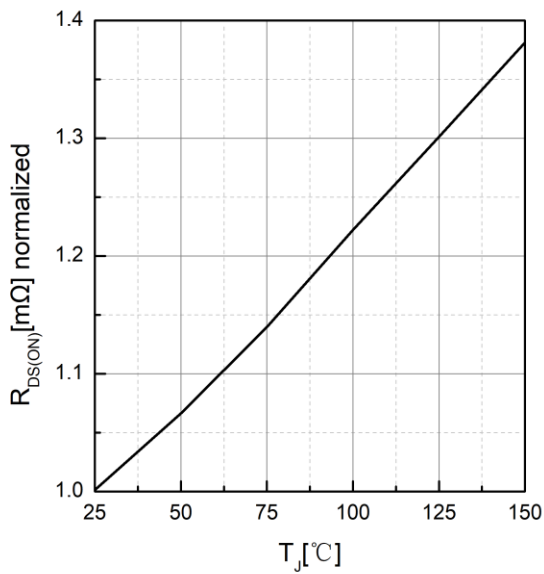
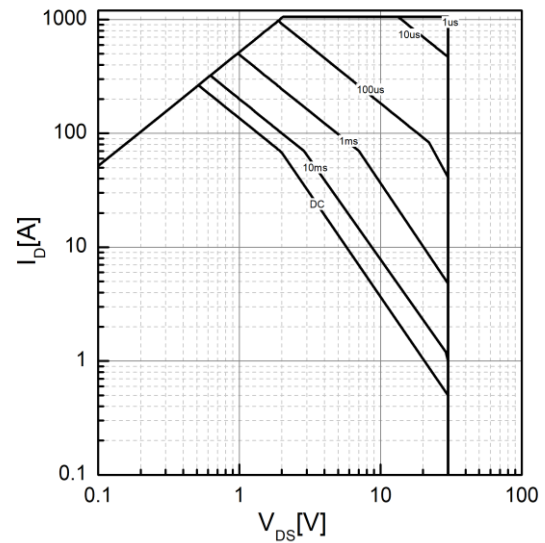
**Electrical Characteristics**  $T_C=25^{\circ}\text{C}$  unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	30	-	-	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS} = 30V, V_{GS} = 0V$	-	-	1	$\mu A$
$I_{GSS}$	Gate to Body Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$	-100	-	100	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0	-	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance <sup>note2</sup>	$V_{GS} = 10V, I_D = 50A$	-	1.40	1.8	m $\Omega$
		$V_{GS} = 4.5V, I_D = 50A$	-	2.20	3.0	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 5V, I_D = 50A$	-	190	-	S
<b>Dynamic Characteristics</b>						
$R_g$	Gate Resistance		-	1.4	-	$\Omega$
$C_{iss}$	Input Capacitance	$V_{DS} = 15V, V_{GS} = 0V,$ $f = 1.0MHz$	-	4300	-	pF
$C_{oss}$	Output Capacitance		-	900	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	830	-	pF
$Q_g$	Total Gate Charge		-	81	-	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS} = 15V, I_D = 20A,$ $V_{GS} = 10V$	-	11	-	nC
$Q_{gd}$	Gate-Drain("Miller") Charge		-	25	-	nC
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15V, I_D = 50A,$ $R_G = 2\Omega, V_{GS} = 10V$	-	19	-	ns
$t_r$	Turn-On Rise Time		-	18	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	47	-	ns
$t_f$	Turn-Off Fall Time		-	19	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Diode Forward Current <sup>note1,5</sup>		-	-	160	A
$I_{SM}$	Maximum Pulsed Diode Forward Current <sup>note2,5</sup>		-	-	1060	A
$t_{rr}$	Reverse Recovery Time	$T_J = 25^{\circ}\text{C}, I_F = 50A$ $di/dt = 150A/\mu s$	-	65	-	ns
$Q_{rr}$	Reverse Recovery Charge	$T_J = 25^{\circ}\text{C}, I_F = 50A$ $di/dt = 150A/\mu s$	-	128	-	nC
$V_{SD}$ <sup>note2</sup>	Drain to Source Diode Forward Voltage	$T_J = 25^{\circ}\text{C}, I_S = 50A,$ $V_{GS} = 0V$	-	0.8	-	V

Note :

- The data tested by surface mounted on one inch<sup>2</sup> FR-4 board with 2OZ copper.
- The data tested by pulsed, pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .
- The EAS data shows Max. rating. The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=95.28A$ .
- The power dissipation is limited by  $150^{\circ}\text{C}$  junction temperature.
- The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.

**Typical Performance Characteristics**

**Figure 1. Output Characteristics,  $T_J=25^\circ\text{C}$** 

**Figure 2. Drain-source on resistance ,  $T_J=25^\circ\text{C}$** 

**Figure 3. Forward characteristics of body diode**

**Figure 4. Gate Charge Characteristics**


**Figure 5. Capacitance Characteristics**

**Figure 6. Threshold Voltage Vs. Temperature**

**Figure 7. Drain-source on-state resistance**

**Figure 8. Maximum Safe Operating Area**

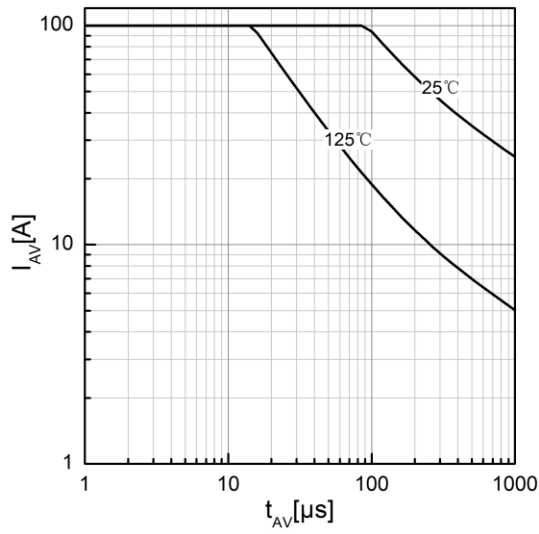


Figure 9. Avalanche characteristics

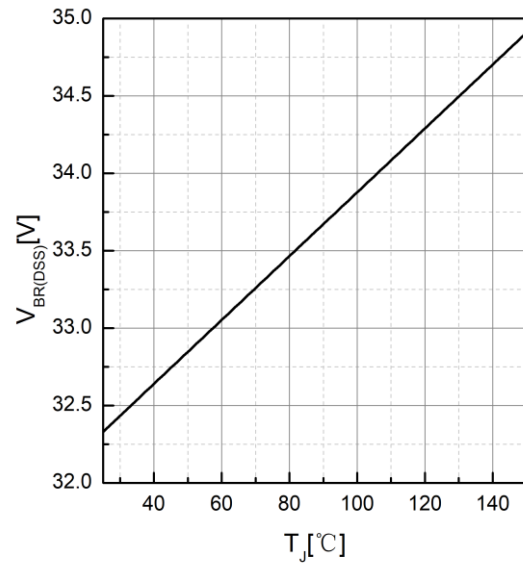


Figure 10. Drain-source breakdown voltage

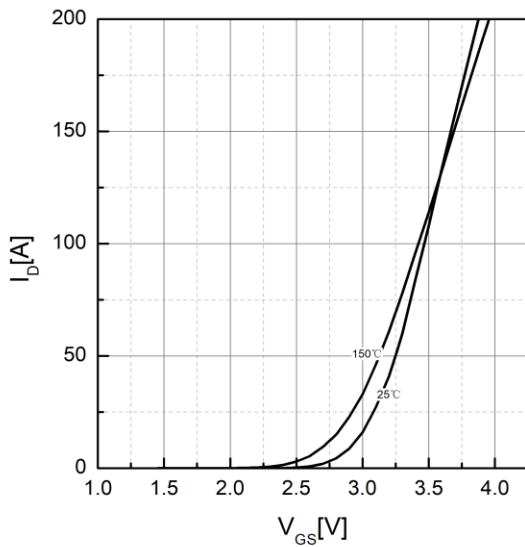


Figure 11. Transfer characteristics

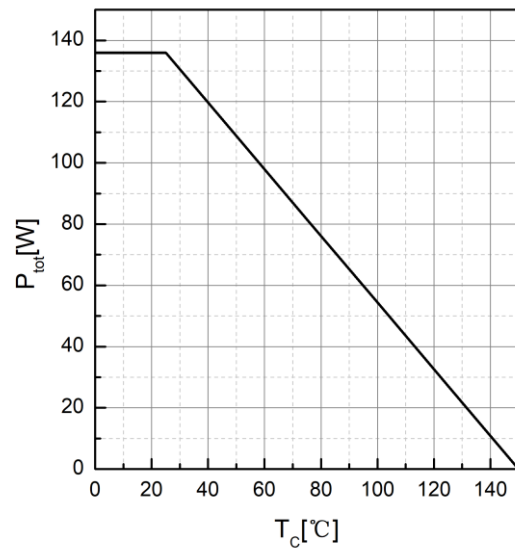
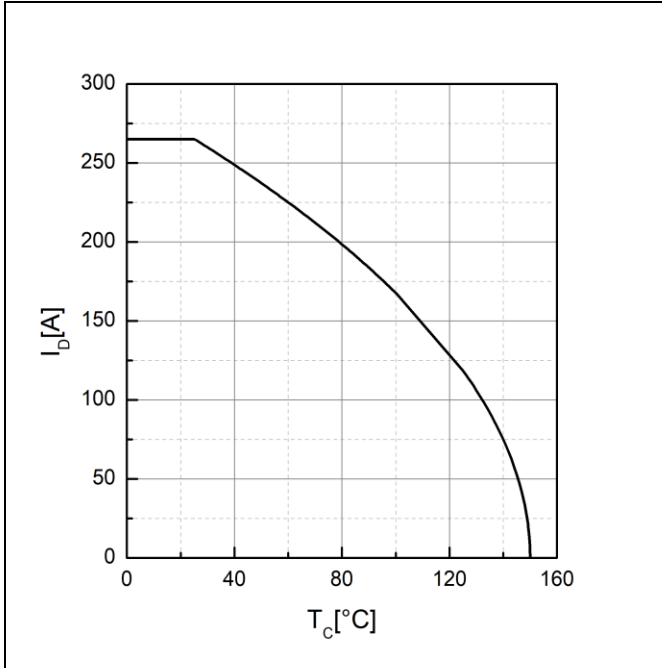
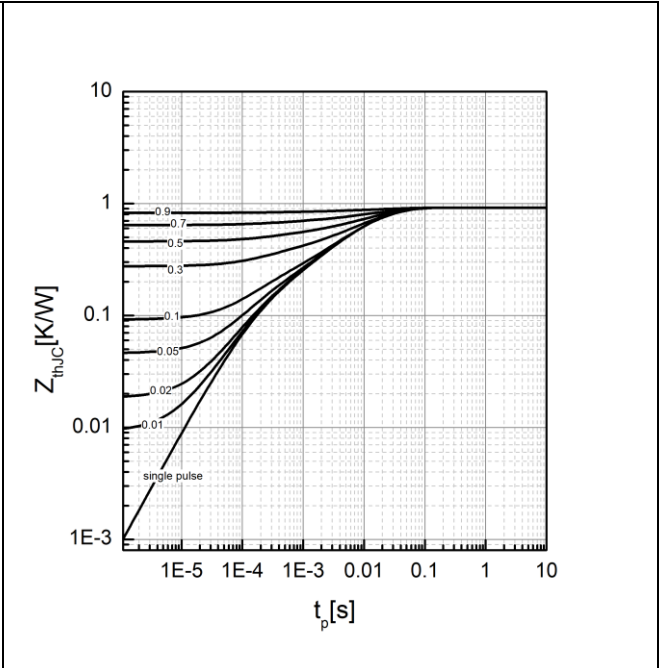


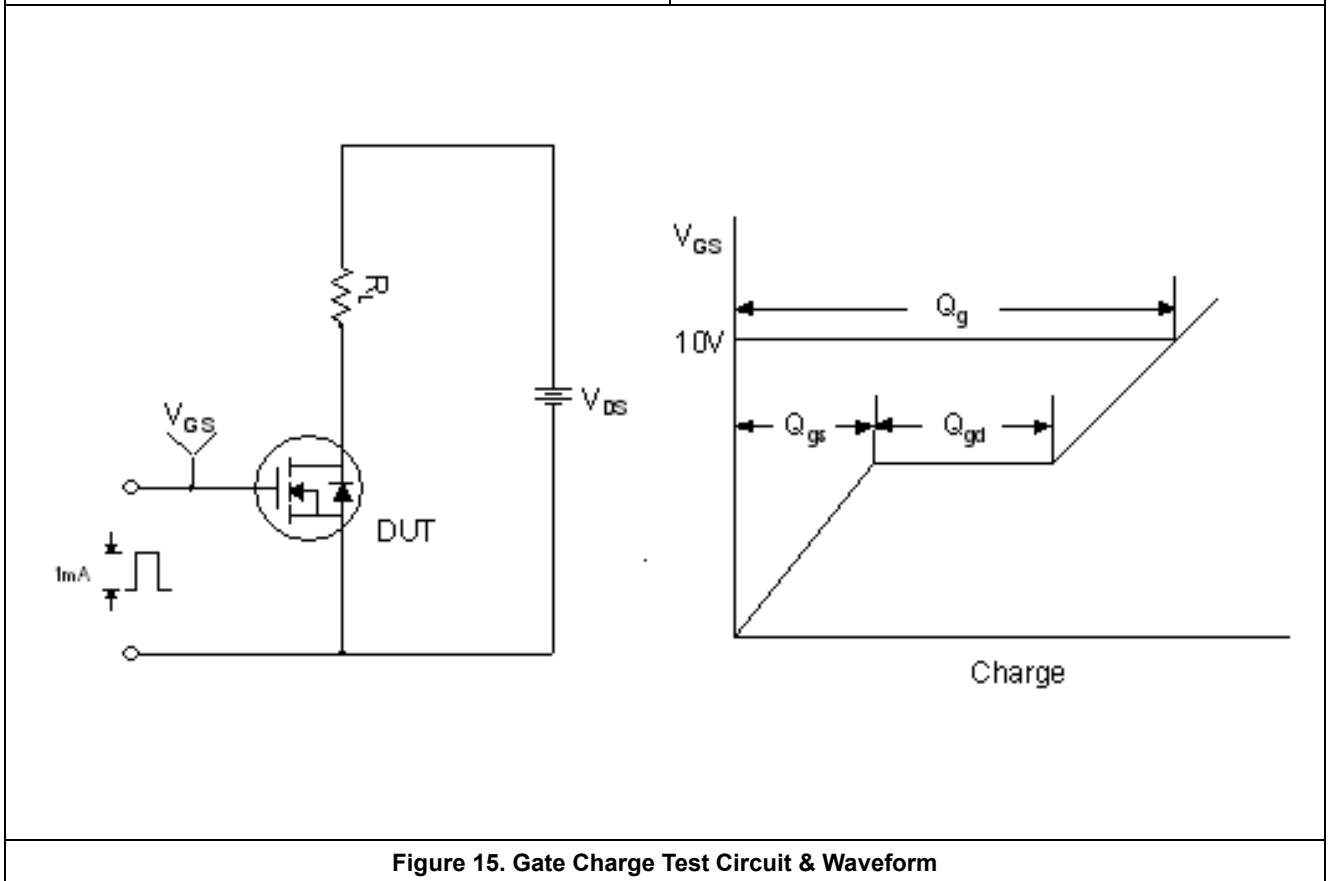
Figure 12. Power dissipation



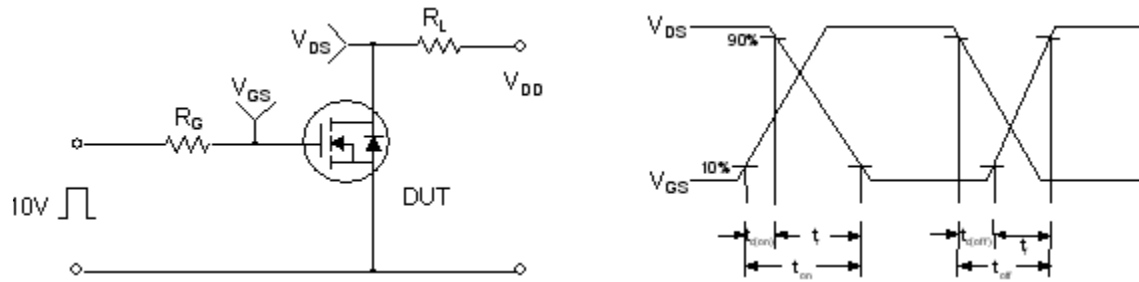
**Figure 13. Drain current**



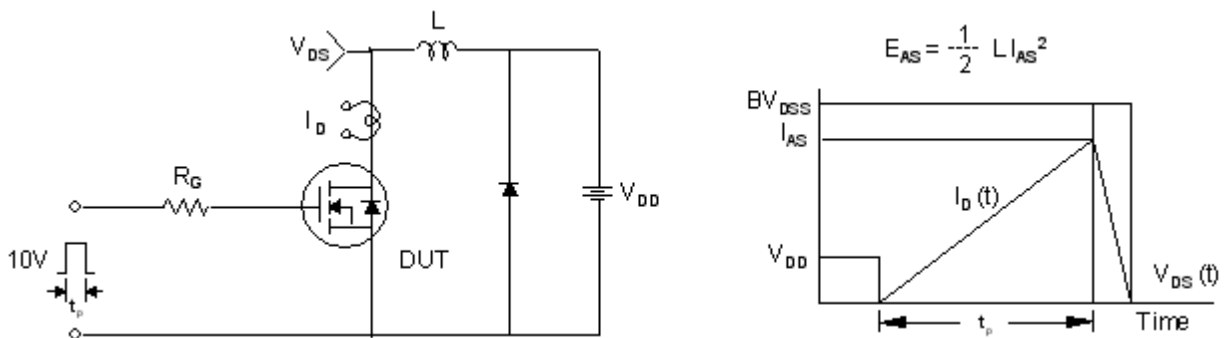
**Figure 14. Effective Transient Thermal Impedance**



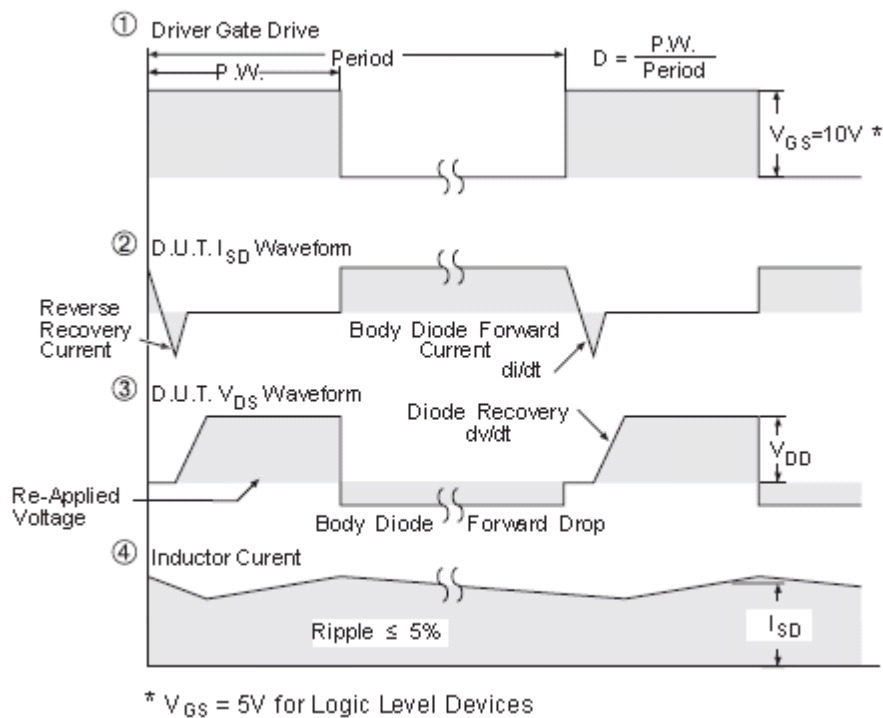
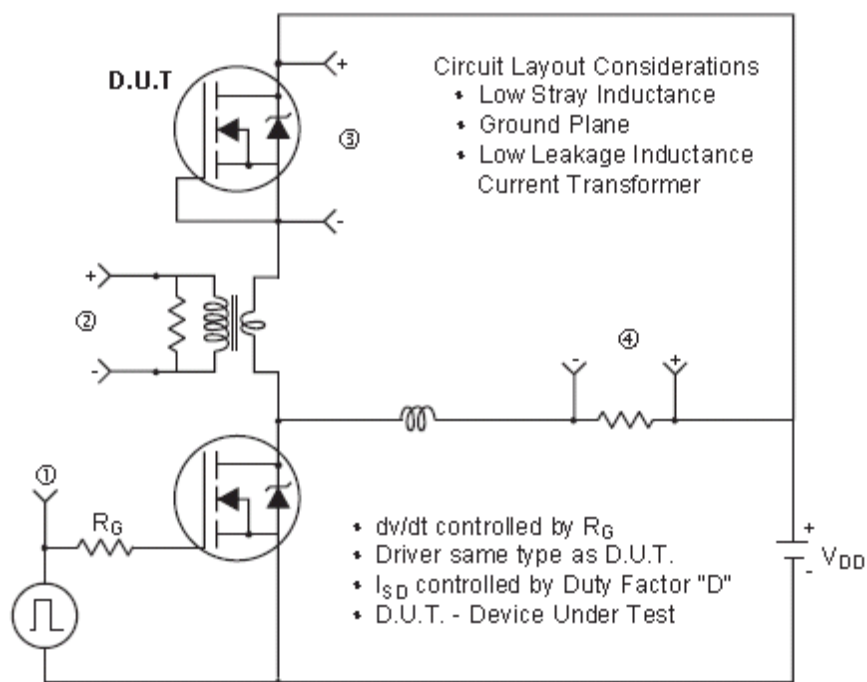
**Figure 15. Gate Charge Test Circuit & Waveform**



**Figure 16. Resistive Switching Test Circuit & Waveforms**

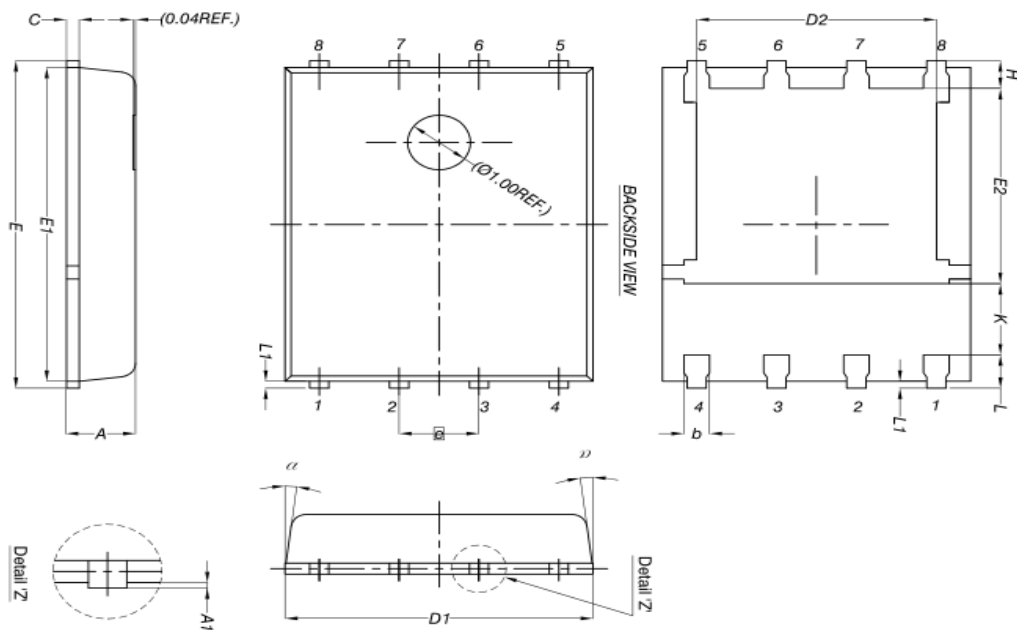


**Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms**

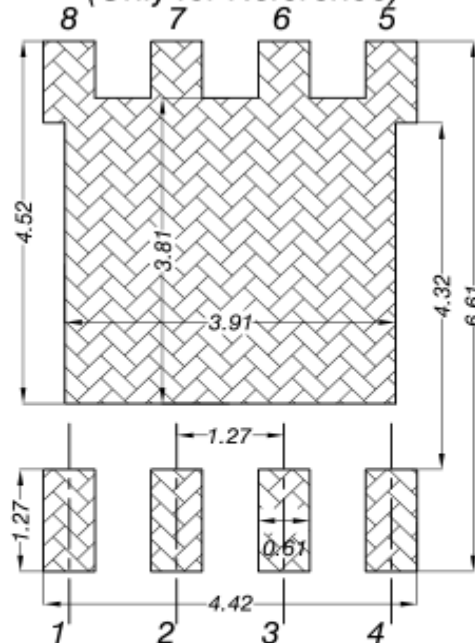


**Figure 18. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms (For N-channel)**



**Package outline**


DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
[e]	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°

**Land Pattern  
(Only for Reference)**

**Note:**

1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs.  
Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar , Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
4. The Package Top May Be Smaller Than The Package Bottom.

**Figure 19. DFN 5x6 Package outline**

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