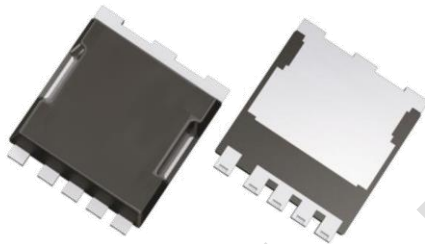


Description
100V N-CHANNEL ENHANCEMENT MODE POWER MOSFET
Features

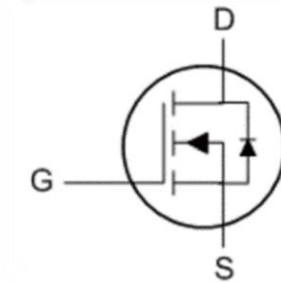
- Device Rating $V_{DS} = 100V$, $I_D = 258A$
- $R_{DS(ON)} = 2.1m\Omega$ (typ.) @ $V_{GS} = 10V$, $I_D = 100A$
- Advanced Split Gate Device Design
- RoHS Compliant & Halogen-Free
- Qualified according to JEDEC for target applications
- 100% avalanche test

Application

- Brushless DC Motor Control
- DC-DC Converters
- Telecom and Server Power Supply
- High Performance Synchronous Rectification
- Load Switch and eFuse

Package


sTOLL
JFG258N100X


Absolute Maximum Ratings $T_C=25^\circ C$ unless otherwise specified

Symbol	Parameter	Max.	Units	
V_{DS}	Drain-Source Voltage	40	V	
V_{GS}	Gate-Source Voltage	± 20	V	
I_D	Continuous Drain Current, $V_{GS} @ 10V$ ^{note1}	$T_C = 25^\circ C$	258	A
		$T_C = 100^\circ C$	163	A
I_{DM}	Pulsed Drain Current ^{note2}	TBD	A	
P_D	Power Dissipation ^{note4}	$T_C = 25^\circ C$	312	W
	Power Dissipation	$T_A = 25^\circ C$	3.1	W
E_{AS}	Single Pulsed Avalanche Energy ^{note3}	TBD	mJ	
$R_{\theta JC}$	Thermal Resistance, Junction to Case ^{note1}	0.4	$^\circ C/W$	
$R_{\theta JA}$	Junction to Ambient (mounted on 1 inch square PCB)	40	$^\circ C/W$	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$	

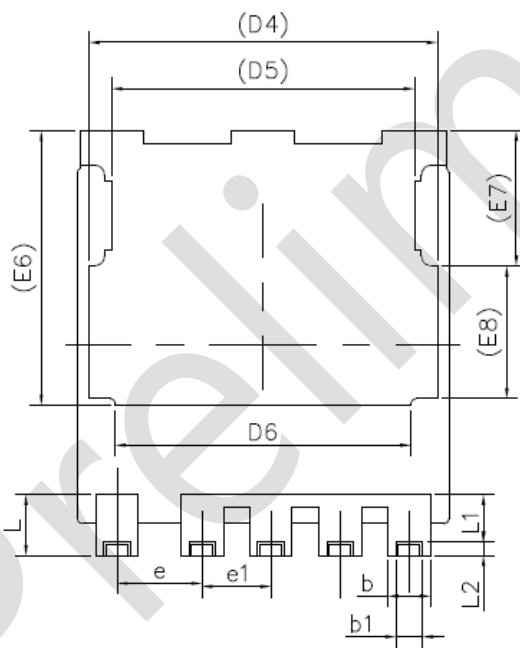
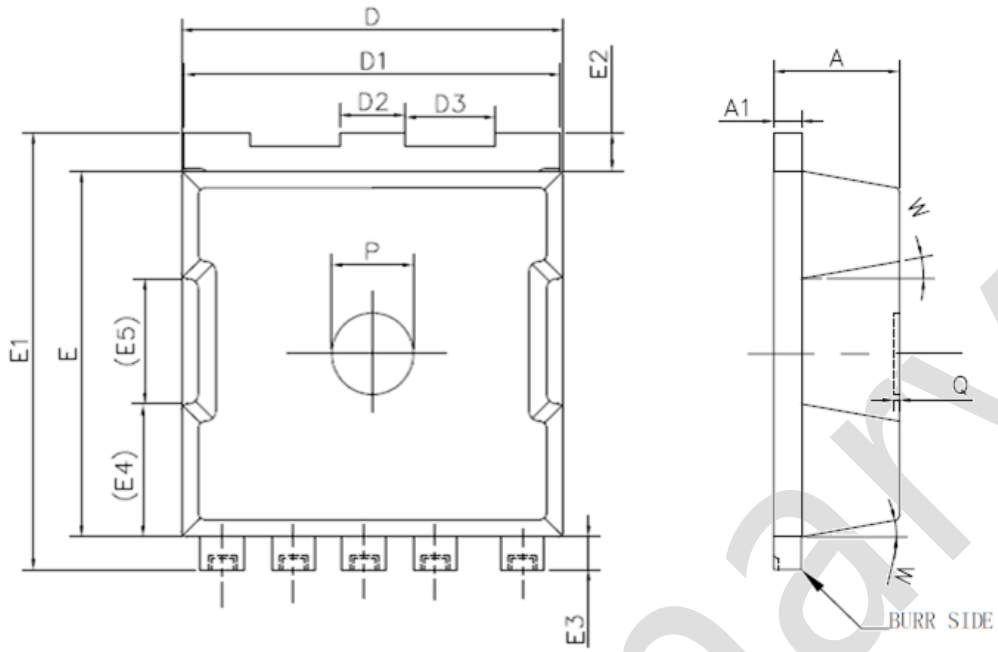
Electrical Characteristics $T_C=25^\circ C$ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	100	-	-	V
I _{DSS}	Drain-Source Leakage Current	V _{DS} = 100V, V _{GS} = 0V, T _C = 25°C	-	-	1	μA
		V _{DS} = 100V, V _{GS} = 0V, T _C = 55°C	-	-	10	μA
I _{GSS}	Gate-Source Leakage Current	V _{DS} = 0V, V _{GS} = ±20V	-100	-	100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2.2	-	3.8	V
R _{DS(on)}	Static Drain-Source On-Resistance ^{note2}	V _{GS} = 10V, I _D = 100A	-	2.1	2.6	mΩ
		V _{GS} = 6V, I _D = 50A	-	TBD	TBD	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 5V, I _D = 100A	-	TBD	-	S
Dynamic Characteristics						
R _g	Gate Resistance		-	TBD	-	Ω
C _{iss}	Input Capacitance	V _{DS} = 50V, V _{GS} = 0V, f = 1MHz	-	4810	-	pF
C _{oss}	Output Capacitance		-	1890	-	pF
C _{rss}	Reverse Transfer Capacitance		-	33	-	pF
Q _g	Total Gate Charge	V _{DS} = 50V, I _D = 100A, V _{GS} = 10V	-	73	-	nC
Q _{gs}	Gate-Source Charge		-	28	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	24	-	nC
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} = 50V, I _D = 100A, R _G = 1Ω, V _{GS} = 10V	-	TBD	-	ns
t _r	Turn-On Rise Time		-	TBD	-	ns
t _{d(off)}	Turn-Off Delay Time		-	TBD	-	ns
t _f	Turn-Off Fall Time		-	TBD	-	ns
Source-Drain Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Diode Forward Current ^{note1,5}		-	-	130	A
I _{SM}	Maximum Pulsed Diode Forward Current ^{note2,5}		-	-	TBD	A
t _{rr}	Reverse Recovery Time	T _J = 25°C, V _R = 50V, I _F = 100A,	-	TBD	-	ns
Q _{rr}	Reverse Recovery Charge	V _{GS} = 0V di/dt = 400A/μs	-	TBD	-	nC
V _{SD} ^{note2}	Source to Drain Diode Forward Voltage	T _J = 25°C, I _S = 100A, V _{GS} = 0V	-	0.8	-	V

Note :

- 1.The data tested by surface mounted on one inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
- 3.The EAS data shows Max. rating. The test condition is L=0.5mH, IAS= TBD A.
- 4.The power dissipation is limited by 150°C junction temperature.
- 5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Package outline



DIMENSION	MILLIMETERS		
	MIN	A	MAX
A	2.20	2.30	2.40
A1	0.40	0.50	0.60
b	0.70	0.80	0.90
b1	0.40	0.50	0.60
D	6.80	7.0	7.20
D1	6.80	6.9	7.20
D2	1.10	1.20	1.30
D3	1.55	1.65	1.75
D4	6.56		
D5	5.70		
D6	5.56		
E	6.50	6.70	6.9
E1	7.80	8.0	8.2
E2	0.60	0.7	0.80
E3	0.50	0.60	0.70
E4	2.43		
E5	2.30		
E6	5.18		
E7	2.55		
E8	2.50		
e	1.60		
e1	1.30		
L	1.05	1.15	1.25
L1	0.80	0.90	1.0
L2	0.15	0.25	0.35
P	1.40	1.50	1.60
Q	0	0.08	0.10
W	8°	10°	11°

Figure 19. sTOLL Package outline
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