

Description

45V N-CHANNEL ENHANCEMENT MODE POWER MOSFET

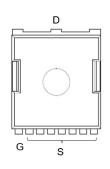
Features

- Device Rating V_{DS} = 45V, I_D = 225A
- $R_{DS(ON)} = 1.5 \text{m}\Omega$ (typ.) @ $V_{GS} = 10 \text{V}$, $I_D = 20 \text{A}$
- $R_{DS(ON)} = 2.0 \text{m}\Omega$ (typ.) @ $V_{GS} = 4.5 \text{V}$, $I_D = 20 \text{A}$
- Proprietary High Density Trench Technology
- RoHS Compliant & Halogen-Free

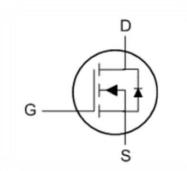
Application

- BMS
- ESS
- PD charger
- E-tool

Package







Absolute Maximum Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter		Max.	Units
V _{DS}	Drain-Source Voltage		45	V
V _{GS}	Gate-Source Voltage		± 20	V
I _D	Continuous Drain Current, VGS @ 10V note1	T _C = 25°C	225	Α
		T _C = 100°C	142	Α
I _{DM}	Pulsed Drain Current note2		900	Α
D-	Power Dissipation note4	T _C = 25°C	138	W
P _D	Power Dissipation	T _A = 25°C	3.12	W
E _{AS}	Single Pulsed Avalanche Energy note3		415	mJ
Rejc	Thermal Resistance, Junction to Case note1		0.9	°C/W
Reja	Junction to Ambient (mounted on 1 inch square PCB)		40	°C/W
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C



Electrical Characteristics Tc=25°C unless otherwise specified

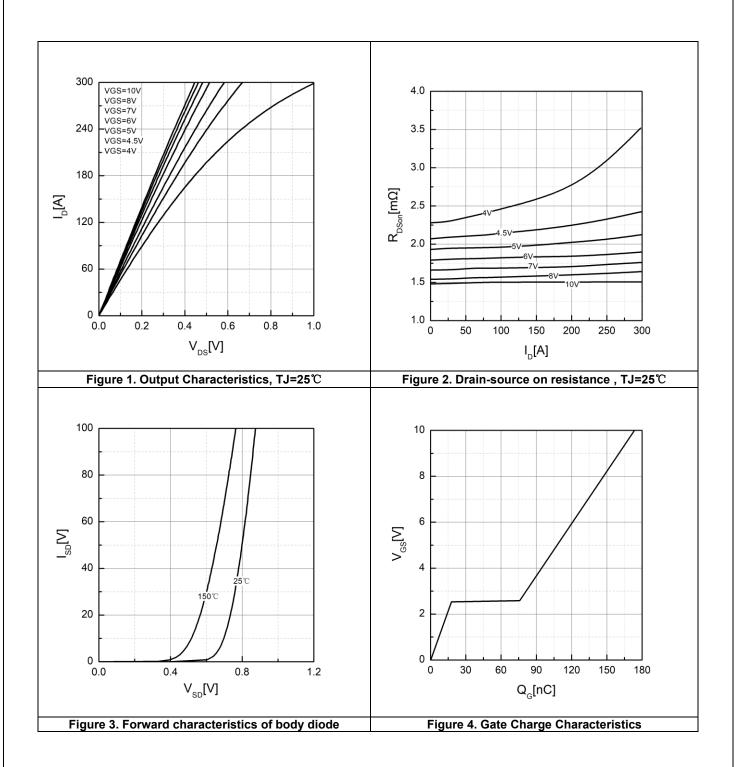
Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Units
Off Charac	teristic					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	45	-	-	V
I _{DSS}	Drain-Source Leakage Current	$V_{DS} = 45V$, $V_{GS} = 0V$, $T_{C} = 25^{\circ}C$	•	-	1	μA
		$V_{DS} = 45V$, $V_{GS} = 0V$, $T_{C} = 55^{\circ}C$	-	-	10	μA
Igss	Gate-Source Leakage Current	$V_{DS} = 0V$, $V_{GS} = \pm 20V$	-100	-	100	nA
On Charac	teristics					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.0	-	2.5	V
D	Static Drain-Source On-Resistance	V _{GS} = 10V, I _D =20A	-	1.5	1.8	mΩ
$R_{DS(on)}$		V _{GS} = 4.5V, I _D =20A	-	2.0	2.4	mΩ
g FS	Forward Transconductance	V _{DS} = 10V, I _D =20A		88	-	S
Dynamic C	haracteristics			•	•	•
Rg	Gate Resistance		-	1.43	-	Ω
Ciss	Input Capacitance	\\ = 20\\ \\ = 0\\	-	7410	-	pF
Coss	Output Capacitance	$V_{DS} = 20V, V_{GS} = 0V,$ f = 1MHz	-	1110	-	pF
Crss	Reverse Transfer Capacitance	1 - 11VII 12	-	1070	-	pF
Q_g	Total Gate Charge	V 00V I 00A	-	173	-	nC
Qgs	Gate-Source Charge	V _{DS} =20V, I _D = 20A, V _{GS} = 10V	-	17.7	-	nC
Q_{gd}	Gate-Drain("Miller") Charge	165 161	-	58	-	nC
Switching	Characteristics					
t _{d(on)}	Turn-On Delay Time		-	40	-	ns
t _r	Turn-On Rise Time	$V_{DD} = 20V, I_D = 20A,$	-	90	-	ns
t _{d(off)}	Turn-Off Delay Time	$R_G = 1\Omega, V_{GS} = 10V$	-	180	-	ns
t _f	Turn-Off Fall Time		-	114	-	ns
Source-Dra	ain Diode Characteristics and Maxin					
Is	Maximum Continuous Diode Forward	d Current note1,5	-	-	115	Α
Ism	Maximum Pulsed Diode Forward Cu	rrent note2,5	-	-	900	Α
t _{rr}	Reverse Recovery Time	$T_J = 25^{\circ}C$, $I_S = 20A$, $V_{GS} = 0V$	-	80	-	ns
Qrr	Reverse Recovery Charge	T _J = 25°C, I _S = 20A, di/dt = 100A/µs		128		nC
V _{SD} note2	Source to Drain Diode Forward Voltage	T _J = 25°C, I _S = 20A, V _{GS} = 0V	_	0.75	-	V

Note:

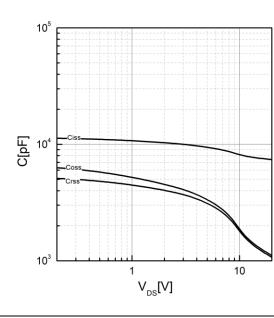
- 1.The data tested by surface mounted on one inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed, pulse width \leq 300us, duty cycle \leq 2%.
- 3. The EAS data shows Max. rating. The test condition is L=0.1 mH, Ias= 91.1 A.
- 4.The power dissipation is limited by 150 $^{\circ}\text{C}\;$ junction temperature.
- 5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.



Typical Performance Characteristics







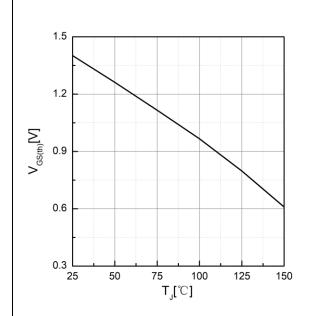


Figure 5. Capacitance Characteristics

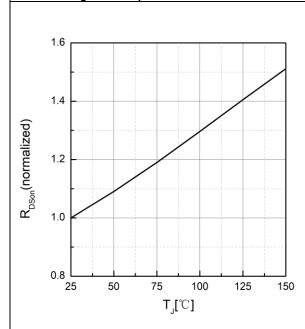


Figure 6. Threshold Voltage Vs. Temperature

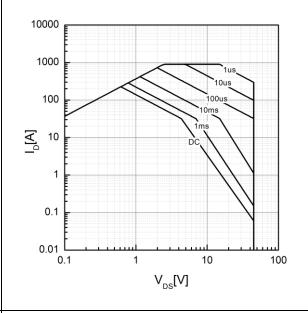
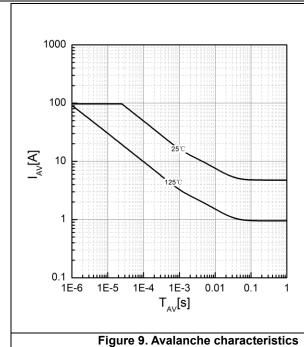
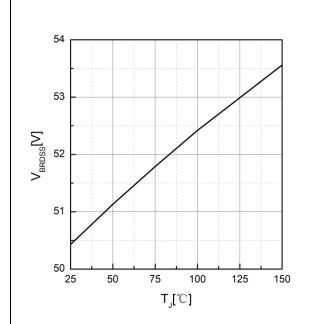


Figure 7. Drain-source on-state resistance

Figure 8. Maximum Safe Operating Area

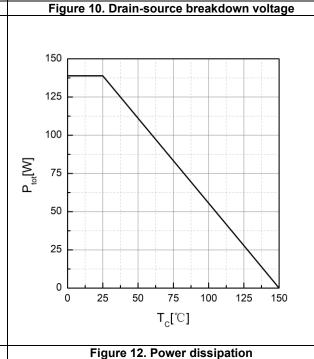




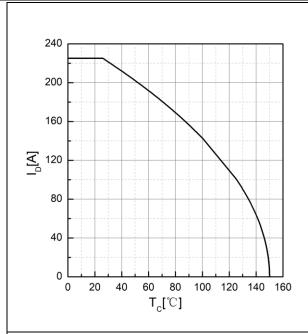


100 80 60 40 20 0 1 2 3 4 5 V_{GS}[V]

Figure 11. Transfer characteristics







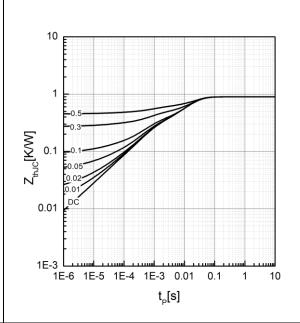
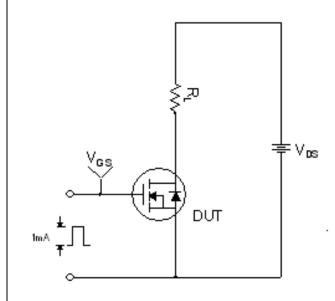


Figure 13. Drain current

Figure 14. Effective Transient Thermal Impedance



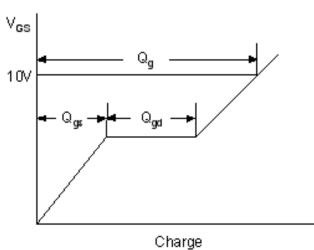
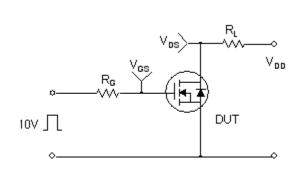
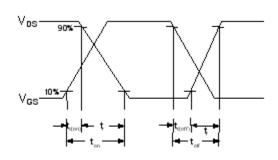
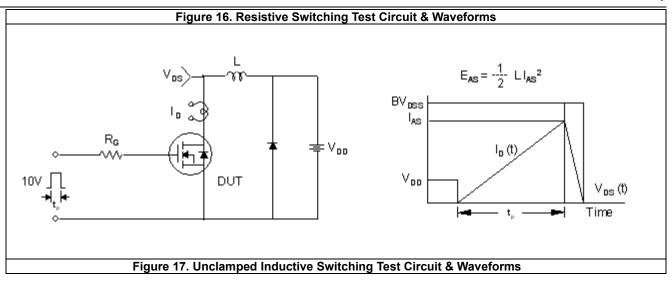


Figure 15. Gate Charge Test Circuit & Waveform

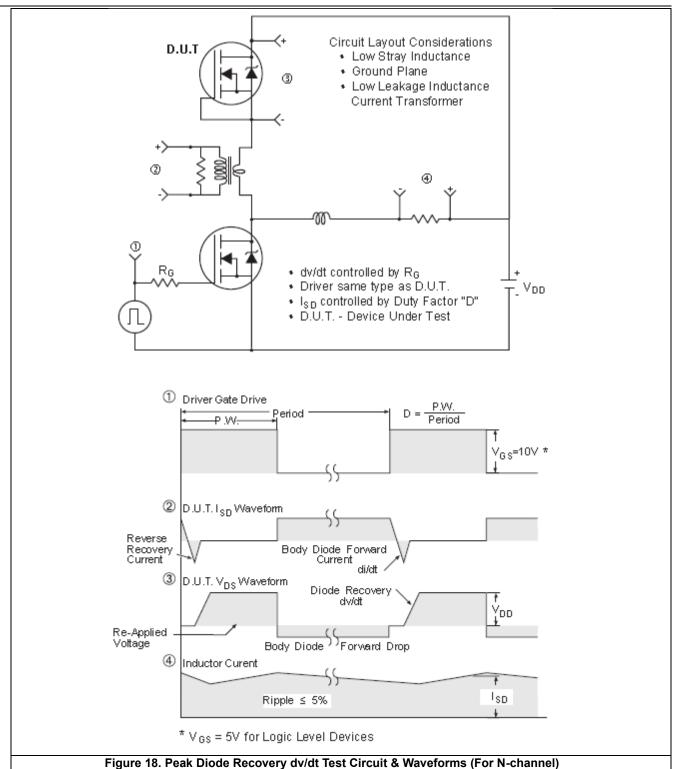






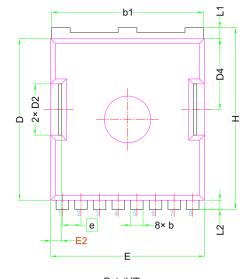


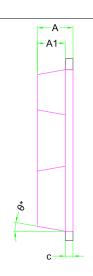


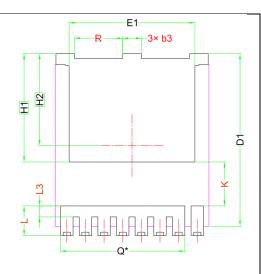




Package outline



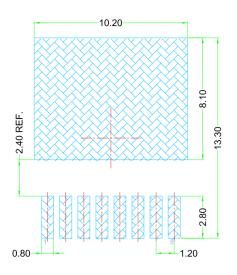








Detail 'Z'



NOTE:

- 1. REFER TO JEDEC MO-299B.
- 2. All DIMENSIONS ARE IN mm, ANGLES IN DEGREES.
- 3. DIMENSIONS DO NOT INCLUSIVE BURRS AND MOLD FLASH.
 4. "*" IS FOR REFERENCE.

SYMBOL	DIMENSIONS			
SIMBOL	MIN.	NOM.	MAX.	
A	2.20	2.30	2.40	
A1	1.70	1.80	1.90	
b	0.70	0.80	0.90	
b1	9.70	9.80	9.90	
b3	1.10	1.20	1.30	
с	0.40	0.50	0.60	
D	10.28	10.38	10.48	
D1	10.98	11.08	11.18	
D2	3.20	3.30	3.40	
D4	4.45	4.55	4.65	
Е	9.80	9.90	1 0.00	
E1	8.00	8.10	8.20	
E2	0.60	0.70	0.80	
e	1.20 BSC			

SYMBOL	DIMENSIONS			
SIMBOL	MIN.	NOM.	MAX.	
Н	11.58	11.68	11.78	
H1	6.95 BSC			
H2	5.89 BSC			
i	0.10 REF.			
j	0.46 REF.			
K	2.80 REF.			
L	1.40	1.90	2.10	
L1	0.60	0.70	0.80	
L2	0.50	0.60	0.70	
L3	0.30	0.70	0.80	
N	8			
Q	8.00 REF.			
R	3.00	3.10	3.20	
θ	10° REF.			

Figure 19. TOLL Package outline



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