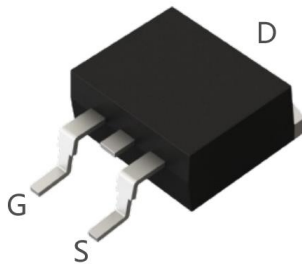


Description
40V N-CHANNEL ENHANCEMENT MODE POWER MOSFET
Features

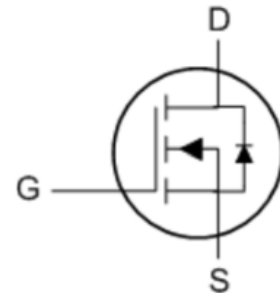
- Device Rating $V_{DS} = 40V$, $I_D = 224A$
- $R_{DS(ON)} = 1.2m\Omega$ (typ.) @ $V_{GS} = 10V$, $I_D = 20A$
- $R_{DS(ON)} = 2.2m\Omega$ (typ.) @ $V_{GS} = 4.5V$, $I_D = 20A$
- Proprietary High Density Trench Technology
- RoHS Compliant & Halogen-Free

Application

- BLDC
- BMS

Package


TO263-3L
JFG224N40E


Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise specified

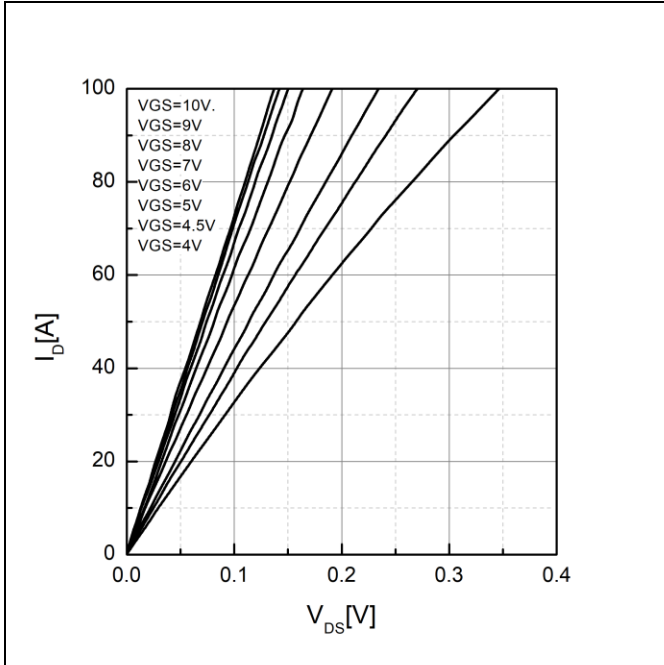
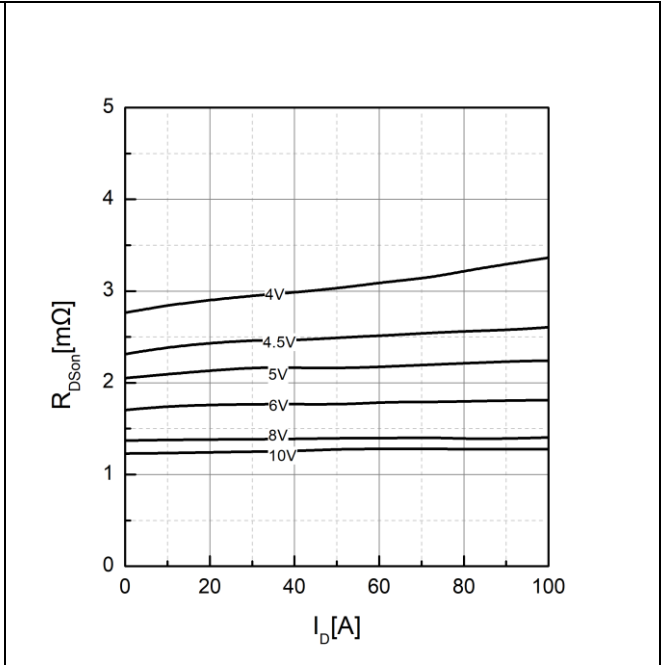
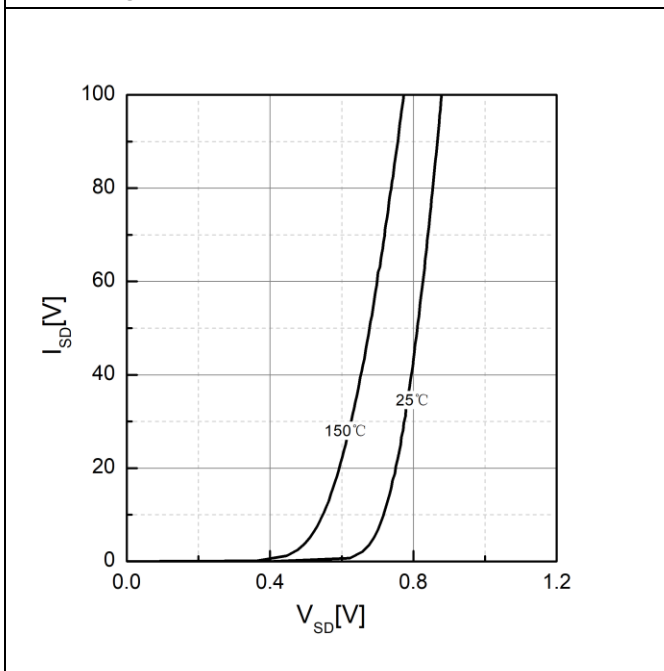
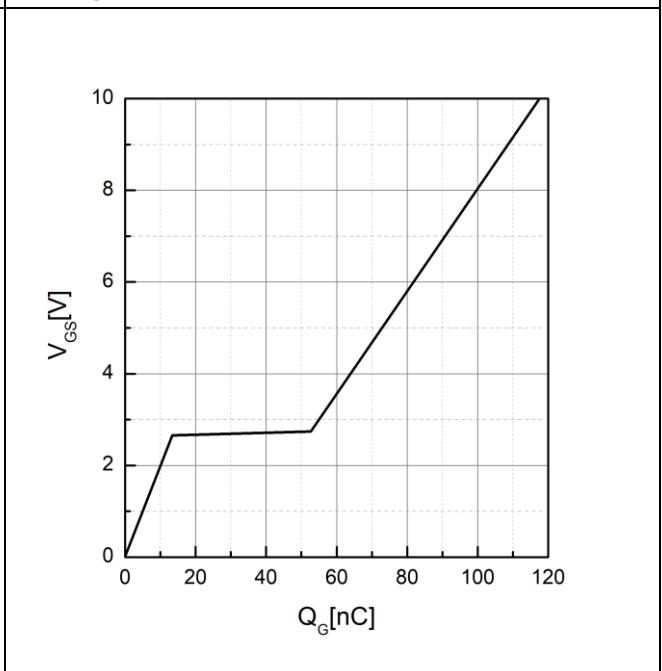
Symbol	Parameter	Max.	Units	
V_{DS}	Drain-Source Voltage	40	V	
V_{GS}	Gate-Source Voltage	± 20	V	
I_D	Continuous Drain Current, $V_{GS} @ 10V$ ^{note1}	$T_C = 25^\circ C$	224	A
		$T_C = 100^\circ C$	142	A
I_{DM}	Pulsed Drain Current ^{note2}	896	A	
P_D	Power Dissipation ^{note4}	$T_C = 25^\circ C$	119	W
	Power Dissipation	$T_A = 25^\circ C$	3.12	W
E_{AS}	Single Pulsed Avalanche Energy ^{note3}	335	mJ	
$R_{\theta JC}$	Thermal Resistance, Junction to Case ^{note1}	1.05	$^\circ C/W$	
$R_{\theta JA}$	Junction to Ambient (mounted on 1 inch square PCB)	40	$^\circ C/W$	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$	

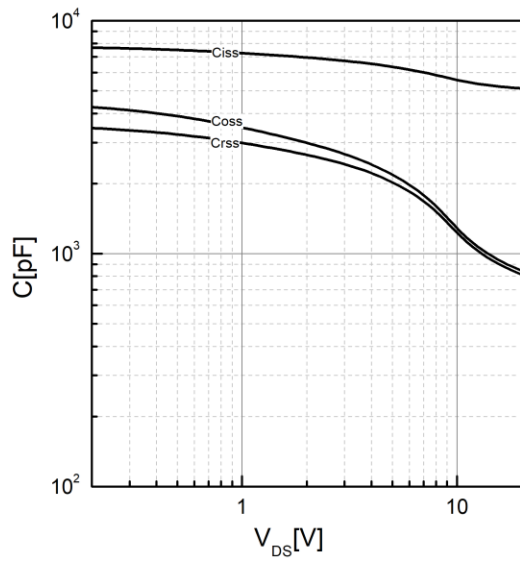
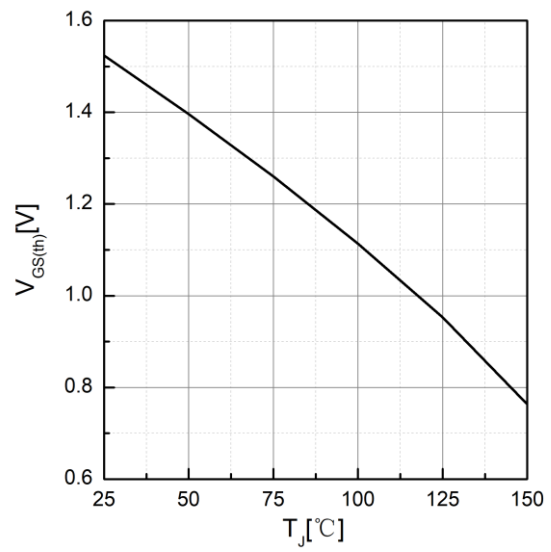
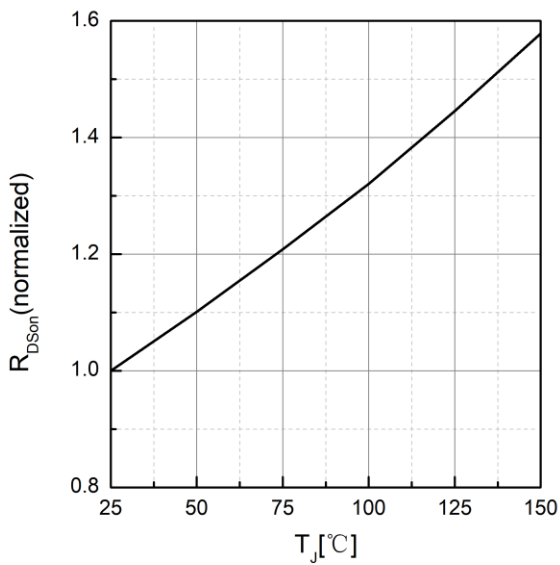
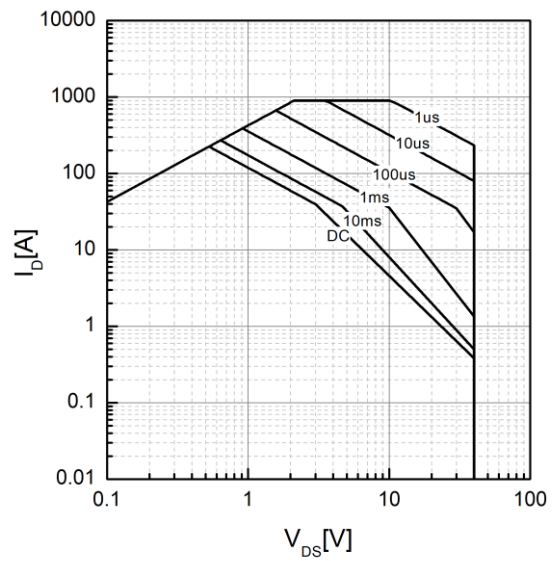
Electrical Characteristics $T_C=25^{\circ}\text{C}$ unless otherwise specified

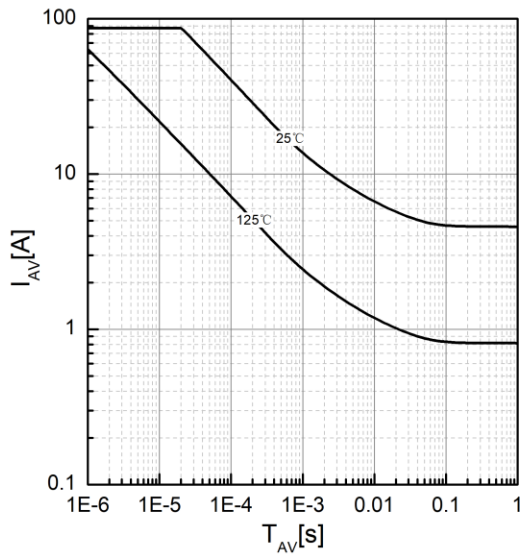
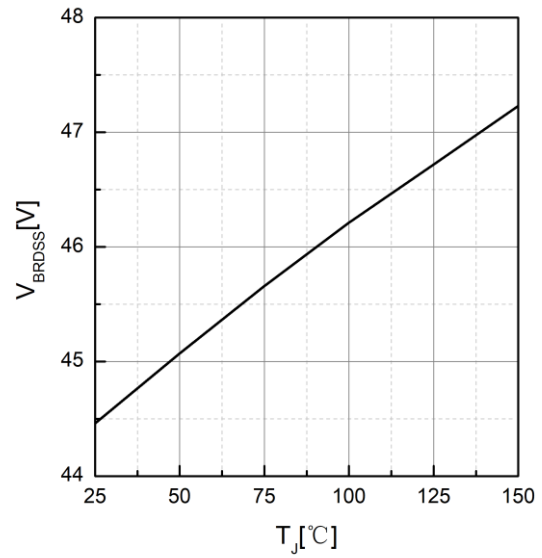
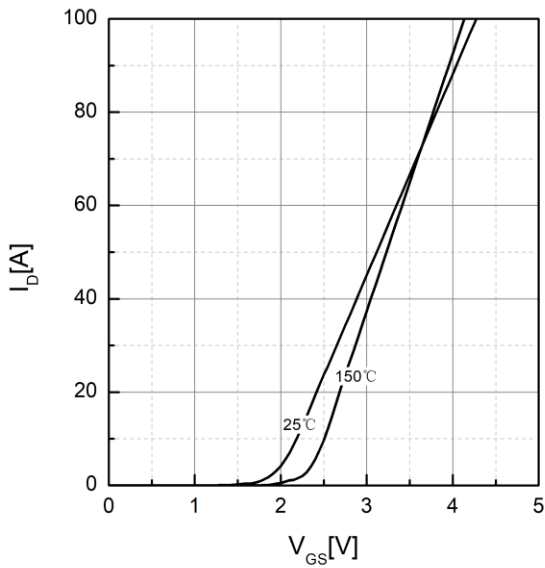
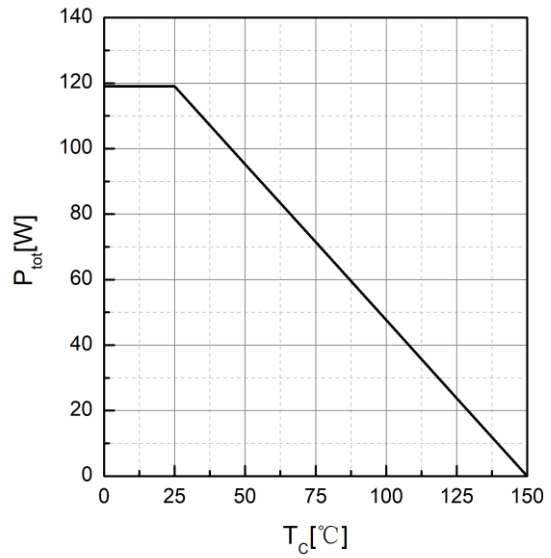
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	40	-	-	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS} = 40V, V_{GS} = 0V, T_C = 25^{\circ}\text{C}$	-	-	1	μA
		$V_{DS} = 40V, V_{GS} = 0V, T_C = 55^{\circ}\text{C}$	-	-	10	μA
I_{GSS}	Gate-Source Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$	-100	-	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0	-	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance <small>note2</small>	$V_{GS} = 10V, I_D = 20A$	-	1.2	1.5	m Ω
		$V_{GS} = 4.5V, I_D = 20A$	-	2.2	2.6	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10V, I_D = 20A$		58	-	S
Dynamic Characteristics						
R_g	Gate Resistance		-	1.3	-	Ω
C_{iss}	Input Capacitance	$V_{DS} = 20V, V_{GS} = 0V,$ $f = 1\text{MHz}$	-	5120	-	pF
C_{oss}	Output Capacitance		-	845	-	pF
C_{rss}	Reverse Transfer Capacitance		-	813	-	pF
Q_g	Total Gate Charge	$V_{DS} = 20V, I_D = 20A,$ $V_{GS} = 10V$	-	117	-	nC
Q_{gs}	Gate-Source Charge		-	13.4	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	39.3	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15V, I_D = 20A,$ $R_G = 1\Omega, V_{GS} = 10V$	-	38	-	ns
t_r	Turn-On Rise Time		-	97	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	200	-	ns
t_f	Turn-Off Fall Time		-	160	-	ns
Source-Drain Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Diode Forward Current <small>note1,5</small>		-	-	99	A
I_{SM}	Maximum Pulsed Diode Forward Current <small>note2,5</small>		-	-	896	A
t_{rr}	Reverse Recovery Time	$T_J = 25^{\circ}\text{C}, I_S = 20A, V_{GS} = 0V$	-	120	-	ns
Q_{rr}	Reverse Recovery Charge	$T_J = 25^{\circ}\text{C}, I_S = 20A,$ $di/dt = 100A/\mu s$		240		nC
V_{SD} <small>note2</small>	Source to Drain Diode Forward Voltage	$T_J = 25^{\circ}\text{C}, I_S = 20A, V_{GS} = 0V$	-	0.77	-	V

Note :

- 1.The data tested by surface mounted on one inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- 3.The EAS data shows Max. rating. The test condition is $L=0.1\text{mH}$, $I_{AS}= 81.8\text{ A}$.
- 4.The power dissipation is limited by 150°C junction temperature.
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Typical Performance Characteristics

Figure 1. Output Characteristics, $T_J=25^\circ\text{C}$

Figure 2. Drain-source on resistance , $T_J=25^\circ\text{C}$

Figure 3. Forward characteristics of body diode

Figure 4. Gate Charge Characteristics


Figure 5. Capacitance Characteristics

Figure 6. Threshold Voltage Vs. Temperature

Figure 7. Drain-source on-state resistance

Figure 8. Maximum Safe Operating Area


Figure 9. Avalanche characteristics

Figure 10. Drain-source breakdown voltage

Figure 11. Transfer characteristics

Figure 12. Power dissipation

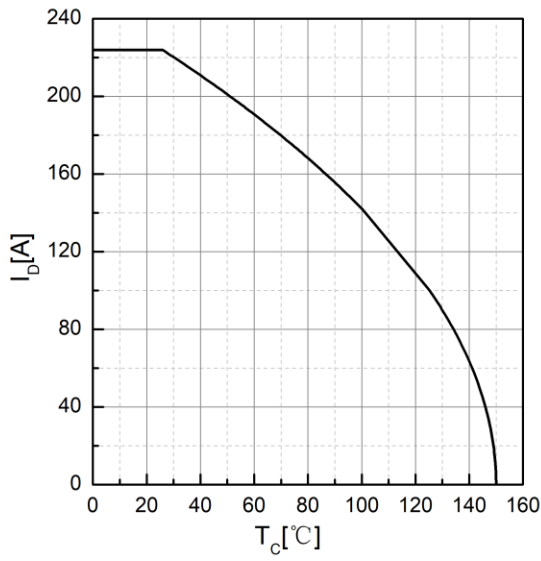


Figure 13. Drain current

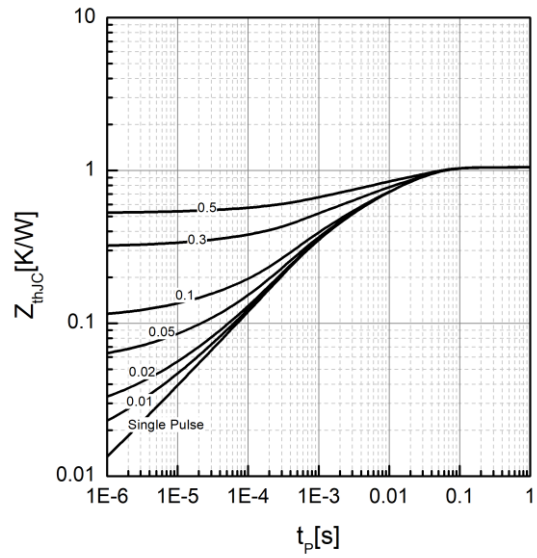


Figure 14. Effective Transient Thermal Impedance

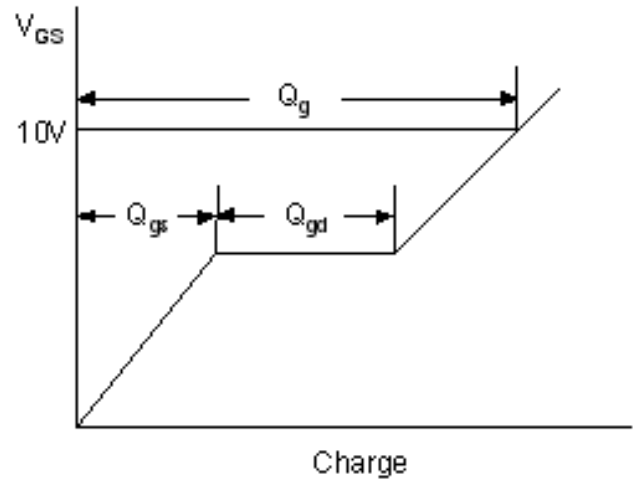
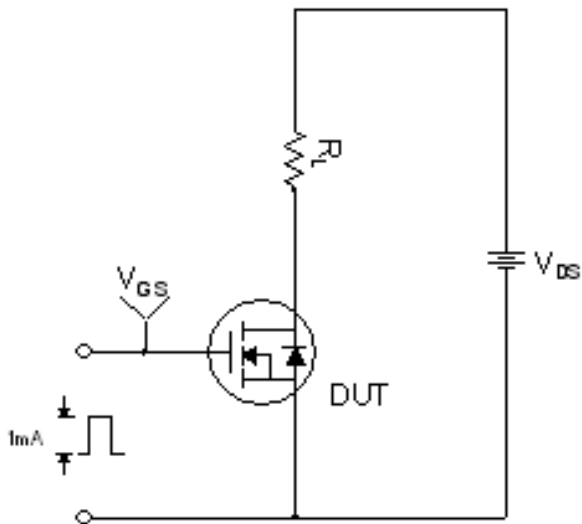


Figure 15. Gate Charge Test Circuit & Waveform

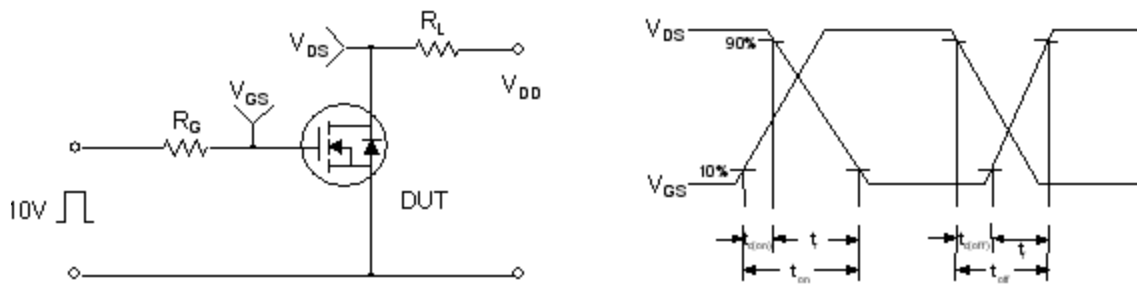


Figure 16. Resistive Switching Test Circuit & Waveforms

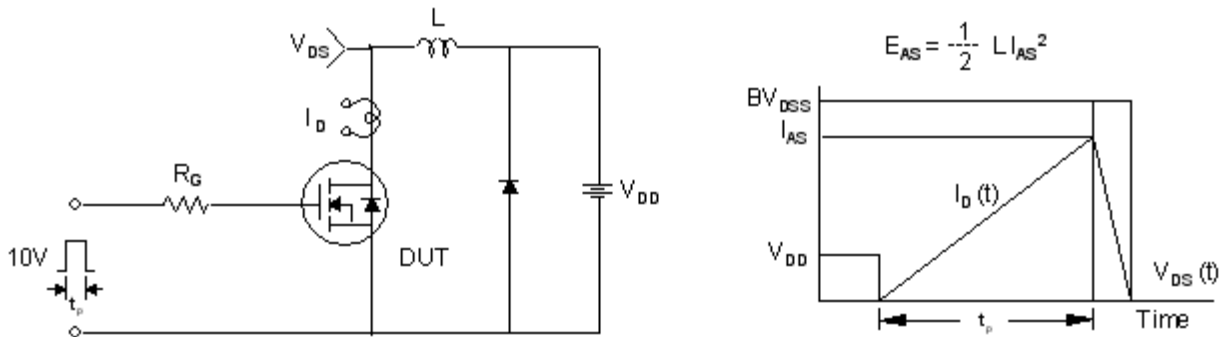


Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms

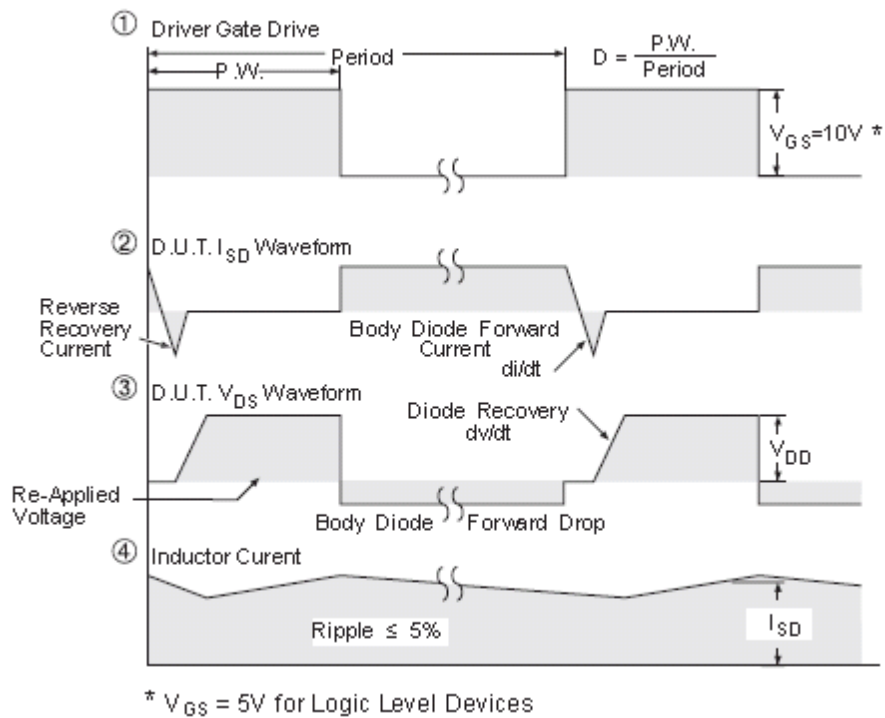
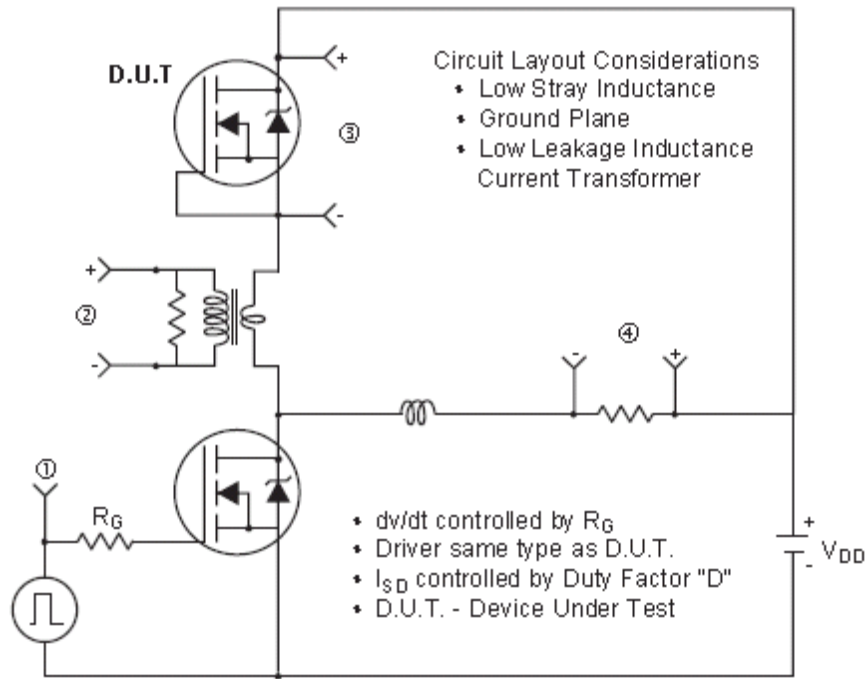
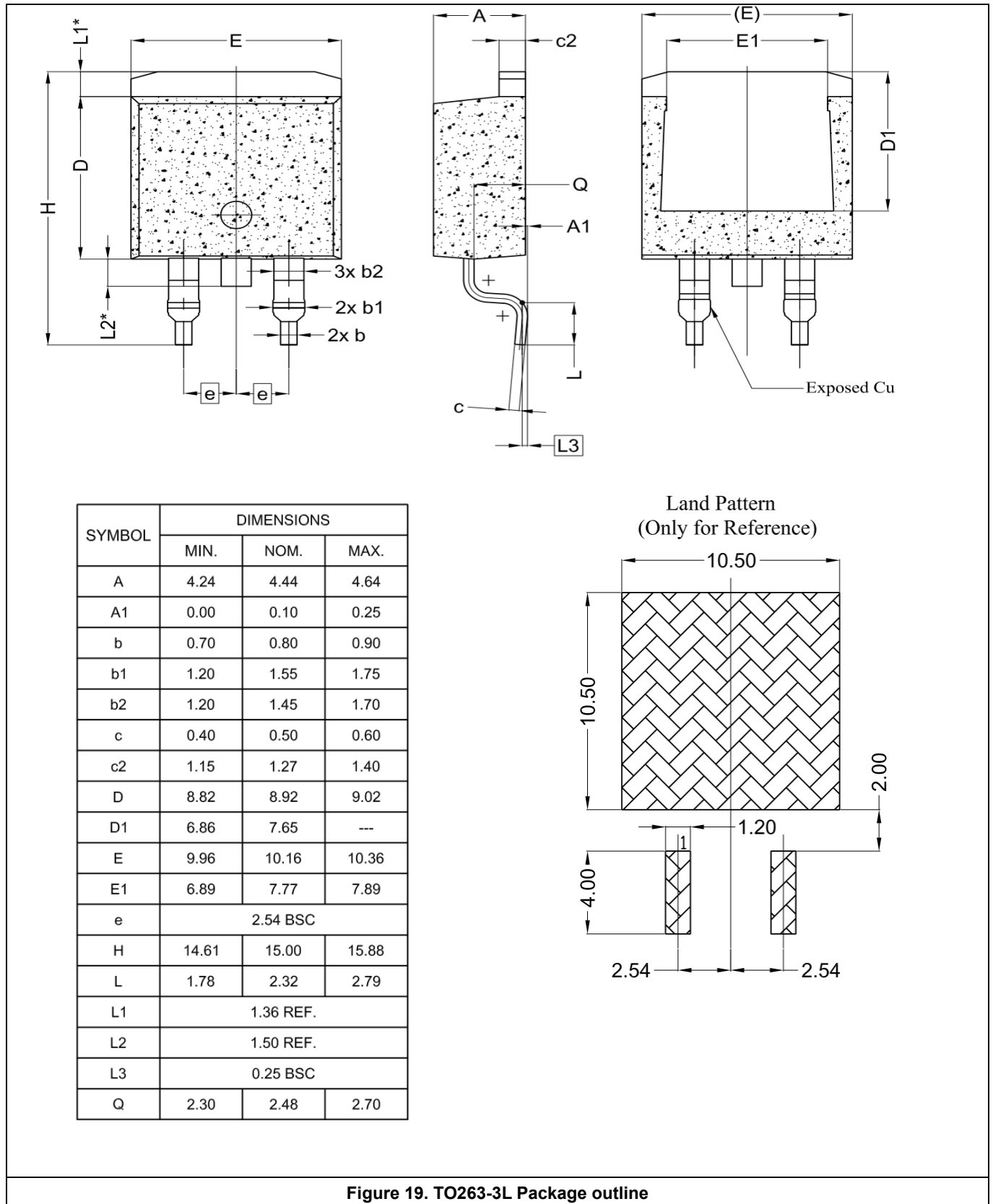


Figure 18. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

Package outline

Figure 19. TO263-3L Package outline

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