Description

40V N-CHANNEL ENHANCEMENT MODE POWER MOSFET

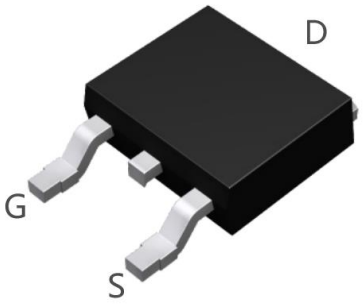
Features

- Device Rating V_{DS} = 40V, I_D = 207A
- $R_{DS(ON)}$ =1.5mΩ (typ.) @ V_{GS} = 10V, I_D = 20A
- $R_{DS(ON)}$ =2.2mΩ (typ.) @ V_{GS} = 4.5V, I_D = 20A
- Proprietary High Density Trench Technology
- RoHS Compliant & Halogen-Free

Application

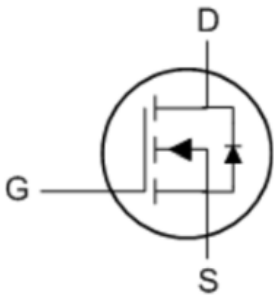
- BLDC
- BMS

Package



TO252-3L

JFG207N40D



Absolute Maximum Ratings T_C=25℃ unless otherwise specified

Symbol	Parameter		Max.	Units
V_{DS}	Drain-Source Voltage		40	V
V_{GS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current, VGS @ 10V note1	T_C = 25℃	207	A
		T_C = 100℃	131	A
I_{DM}	Pulsed Drain Current note2		828	A
P_D	Power Dissipation note4	T_C = 25℃	113	W
	Power Dissipation	T_A = 25℃	3.12	W
E_{AS}	Single Pulsed Avalanche Energy note3		291	mJ
$R_{\theta JC}$	Thermal Resistance, Junction to Case note1		1.1	℃/W
$R_{\theta JA}$	Junction to Ambient (mounted on 1 inch square PCB)		40	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

Electrical Characteristics T_C=25℃ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	40	-	-	V
I_{DSS}	Drain-Source Leakage Current	V_{DS} = 40V, V_{GS} = 0V, T_C = 25℃	-	-	1	μA
		V_{DS} = 40V, V_{GS} = 0V, T_C = 55℃	-	-	10	μA
I_{GSS}	Gate-Source Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-100	-	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1.0	-	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance note2	V_{GS} = 10V, I_D =20A	-	1.5	1.8	mΩ
		V_{GS} = 4.5V, I_D =20A	-	2.2	2.7	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10V, I_D =20A		85	-	S
Dynamic Characteristics						
R_g	Gate Resistance		-	1.4	-	Ω
C_{iss}	Input Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz	-	4980	-	pF
C_{oss}	Output Capacitance		-	896	-	pF
C_{rss}	Reverse Transfer Capacitance		-	861	-	pF
Q_g	Total Gate Charge	V_{DS} =20V, I_D = 20A, V_{GS} = 10V	-	119	-	nC
Q_{gs}	Gate-Source Charge		-	11.6	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	42	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 20V, I_D = 20A, R_G = 1Ω, V_{GS} = 10V	-	30	-	ns
t_r	Turn-On Rise Time		-	70	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	130	-	ns
t_f	Turn-Off Fall Time		-	86	-	ns
Source-Drain Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Diode Forward Current note1,5		-	-	94	A
I_{SM}	Maximum Pulsed Diode Forward Current note2,5		-	-	828	A
t_{rr}	Reverse Recovery Time	T_J = 25°C, I_S = 20A, V_{GS} = 0V	-	70	-	ns
Q_{rr}	Reverse Recovery Charge	T_J = 25°C, I_S = 20A, di/dt = 100A/μs		112		nC
V_{SD} note2	Source to Drain Diode Forward Voltage	T_J = 25°C, I_S = 20A, V_{GS} = 0V	-	0.77	-	V

Note :

1.The data tested by surface mounted on one $inch^2$ FR-4 board with 2OZ copper.

2.The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.

3.The EAS data shows Max. rating. The test condition is L=0.1mH, I_{AS}= 76.3 A.

4.The power dissipation is limited by 150℃ junction temperature.

5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Performance Characteristics

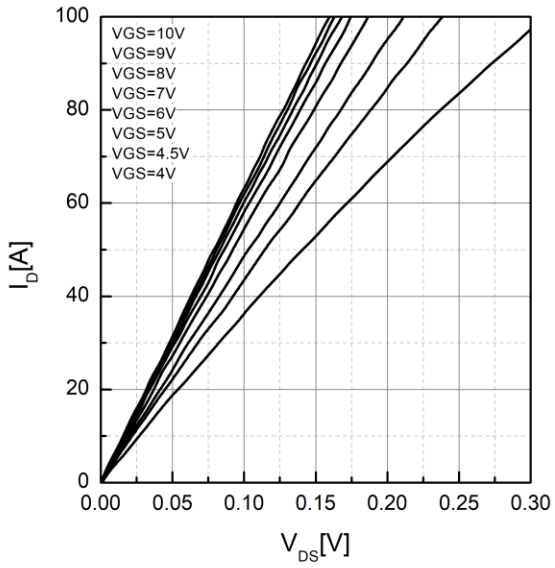


Figure 1. Output Characteristics, TJ=25℃

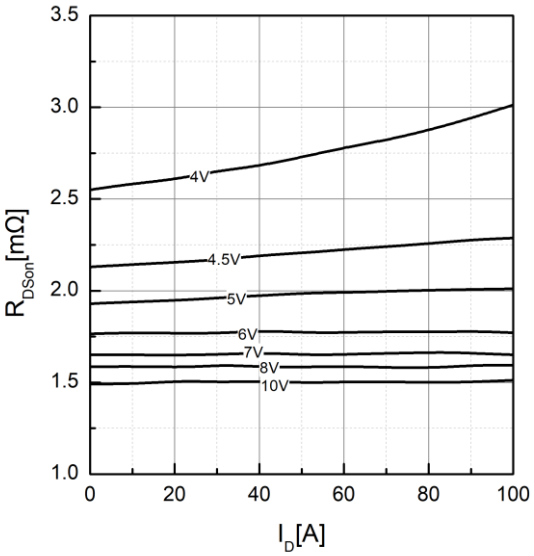


Figure 2. Drain-source on resistance , TJ=25℃

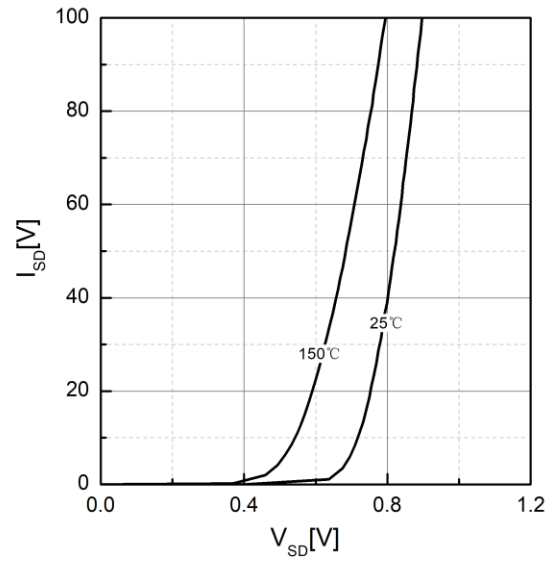


Figure 3. Forward characteristics of body diode

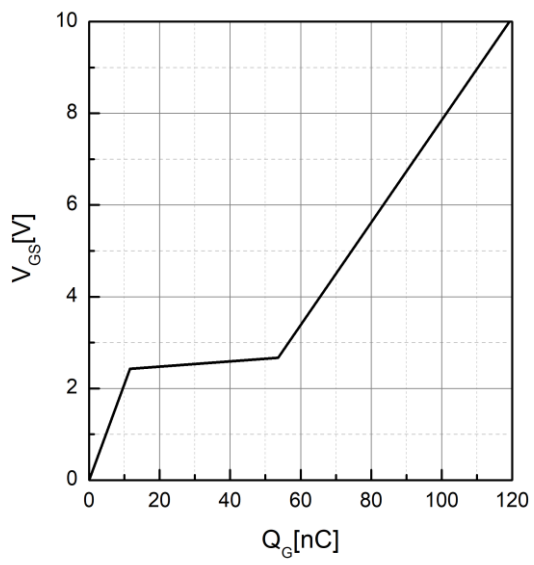


Figure 4. Gate Charge Characteristics

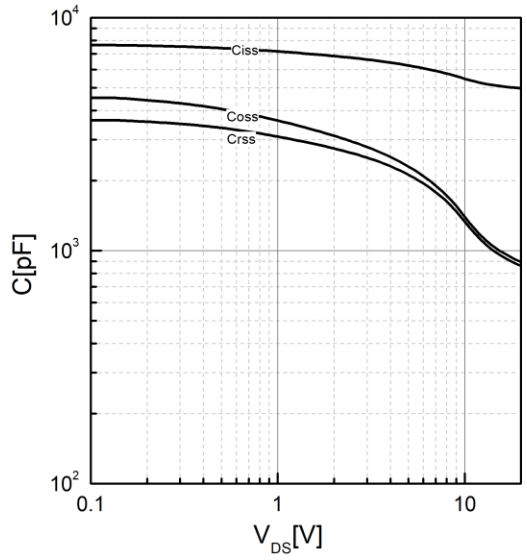


Figure 5. Capacitance Characteristics

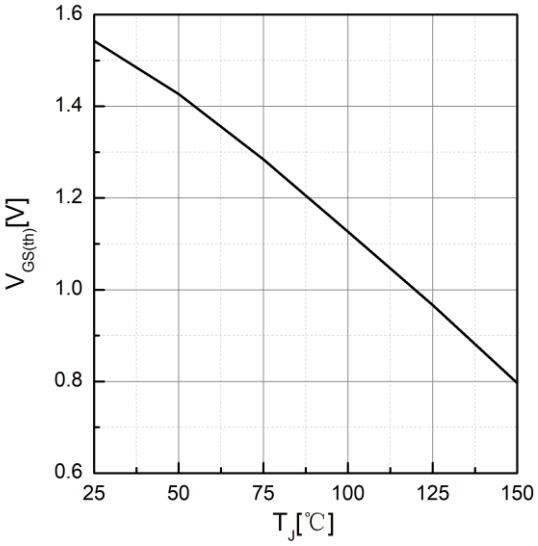


Figure 6. Threshold Voltage Vs. Temperature

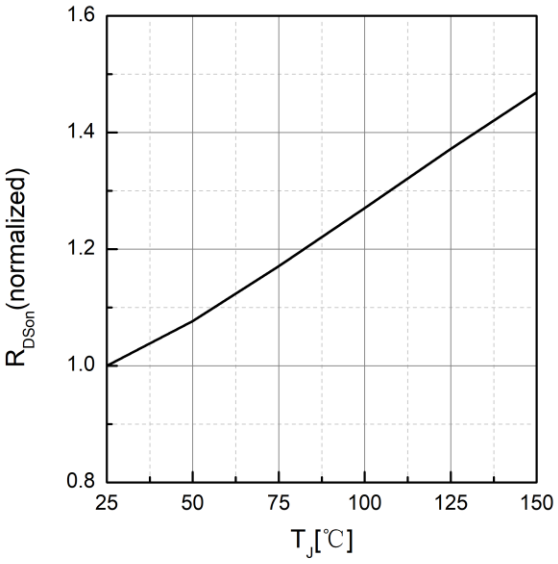


Figure 7. Drain-source on-state resistance

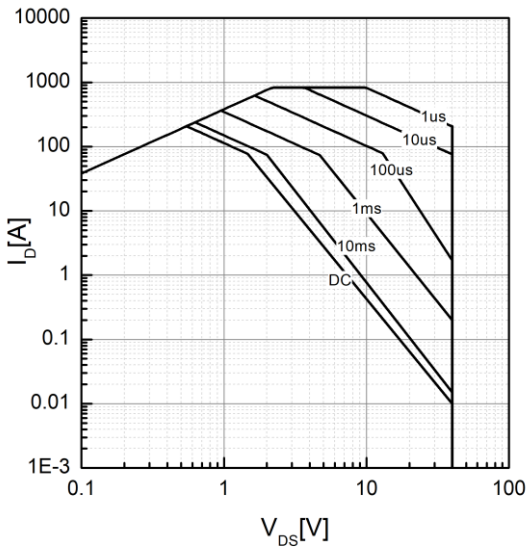


Figure 8. Maximum Safe Operating Area

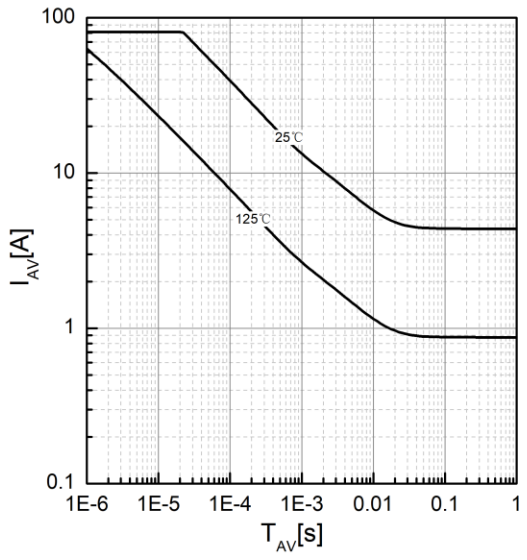


Figure 9. Avalanche characteristics

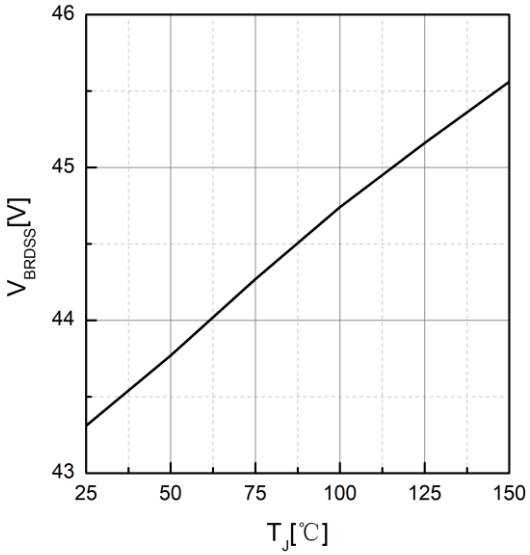


Figure 10. Drain-source breakdown voltage

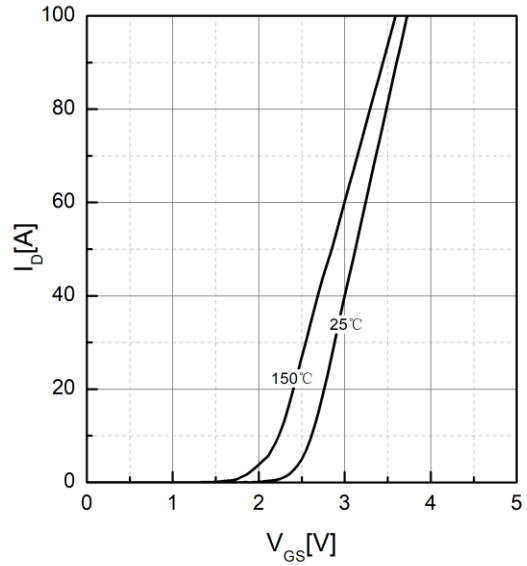


Figure 11. Transfer characteristics

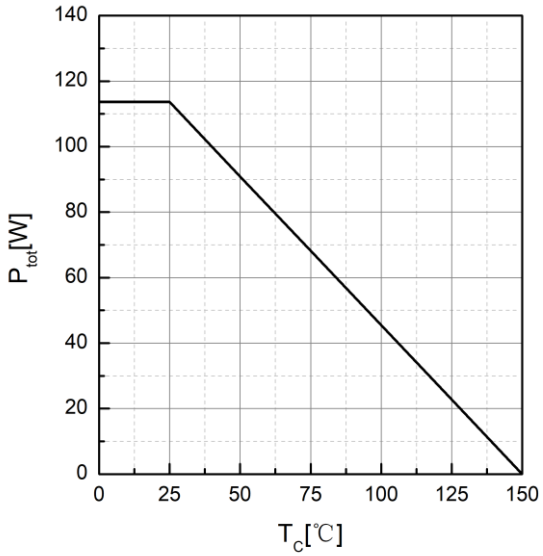


Figure 12. Power dissipation

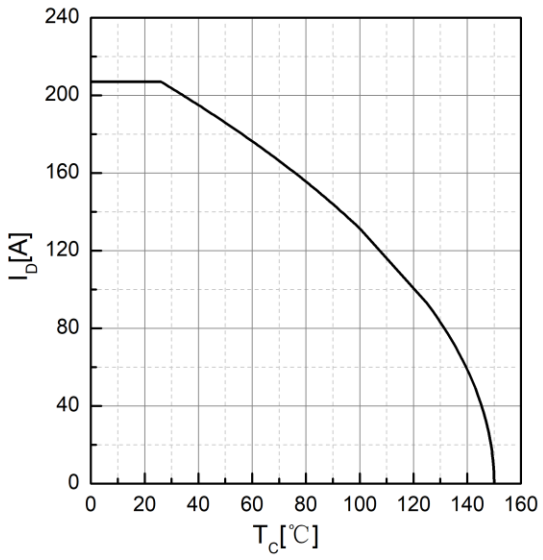


Figure 13. Drain current

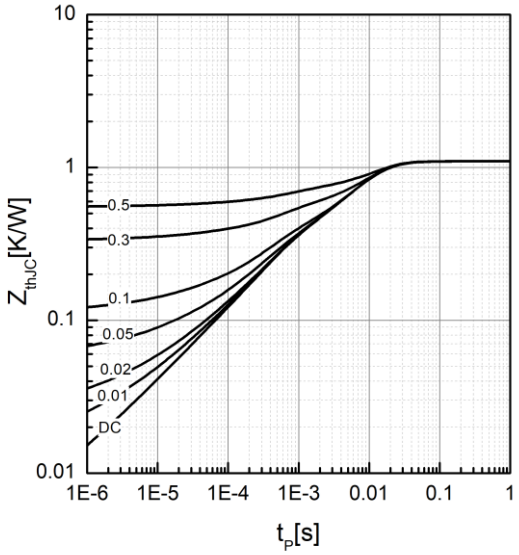


Figure 14. Effective Transient Thermal Impedance

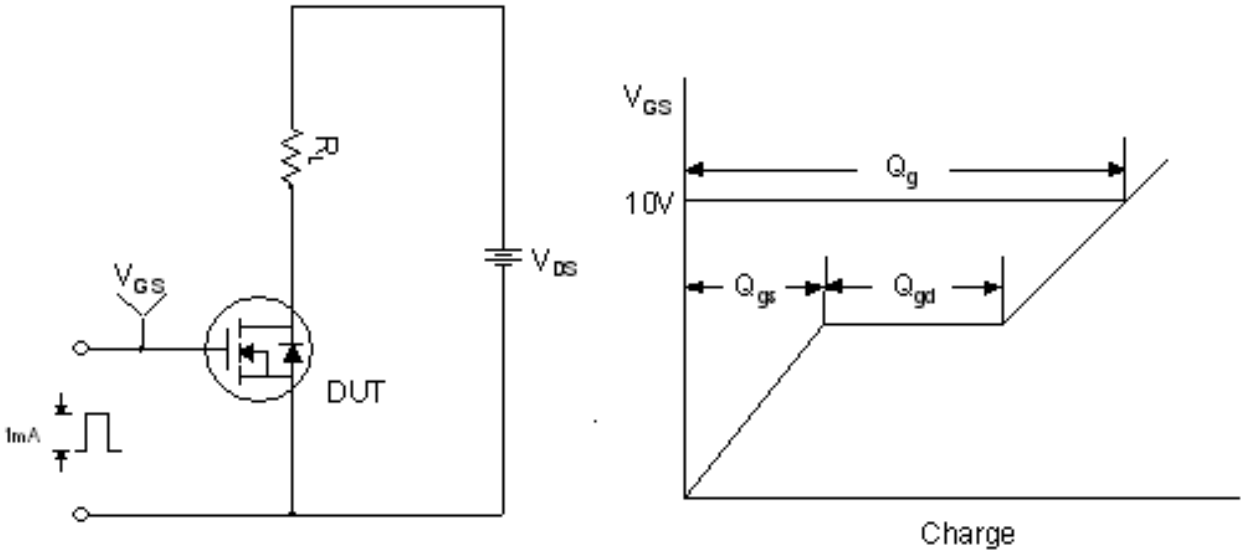


Figure 15. Gate Charge Test Circuit & Waveform

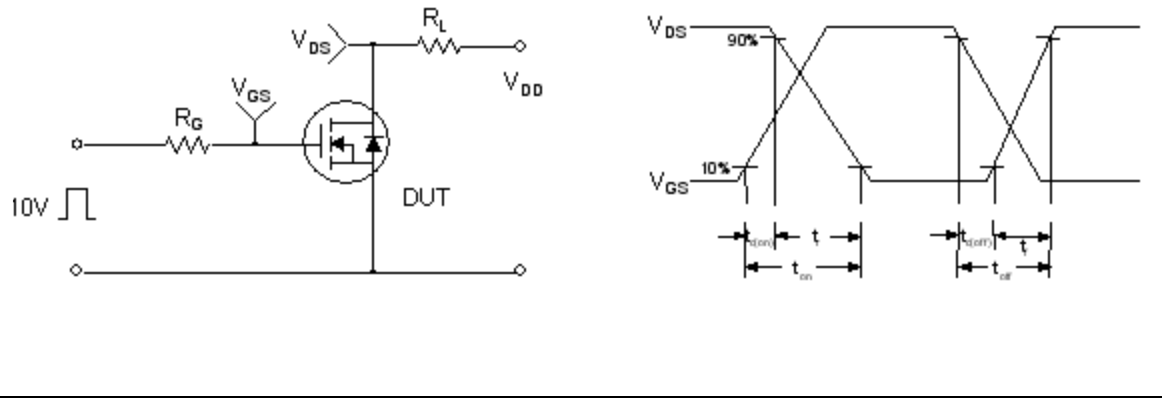


Figure 16. Resistive Switching Test Circuit & Waveforms

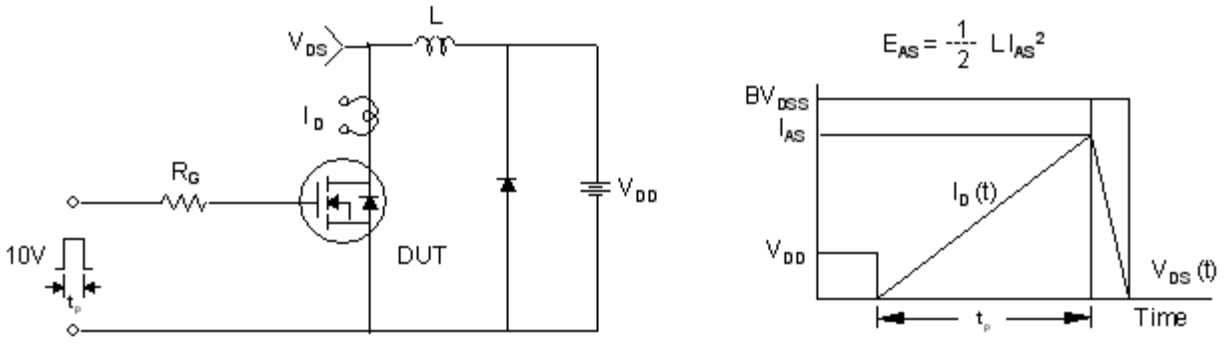


Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms

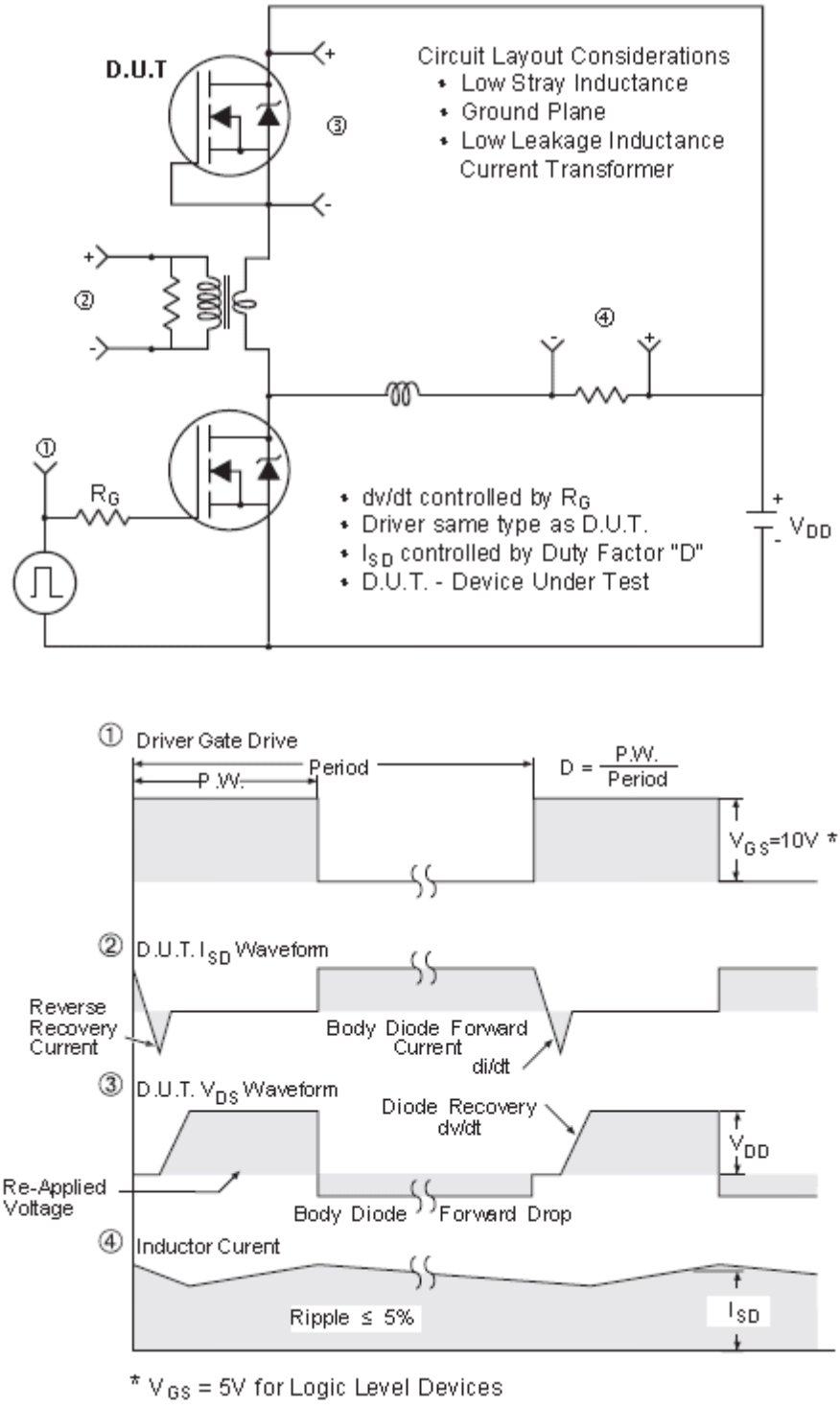
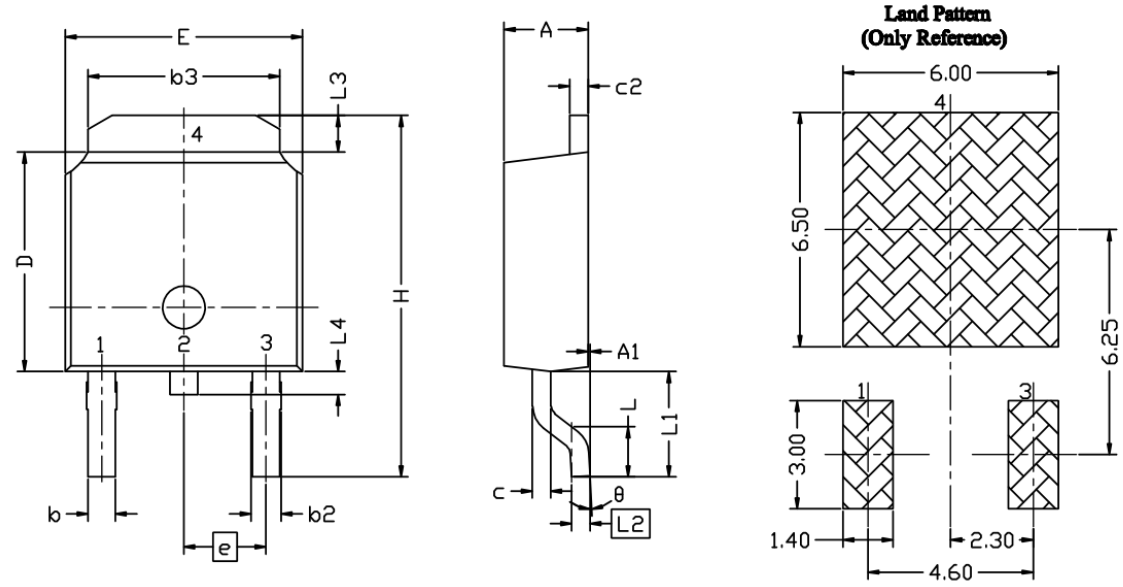
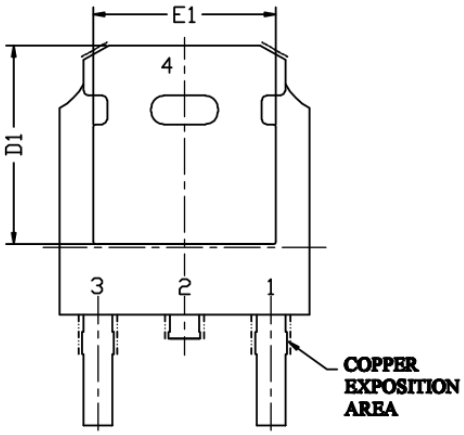


Figure 18. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

Package outline





SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
E	6.40	6.60	6.731
L	1.40	1.52	1.77
L1	2.743 REF		
L2	0.508 BSC		
L3	0.89	--	1.27
L4	0.64	--	1.01
D	6.00	6.10	6.223
H	9.40	10.00	10.40
b	0.64	0.76	0.88
b2	0.77	0.84	1.14
b3	5.21	5.34	5.46
e	2.286 BSC		
A	2.20	2.30	2.38
A1	0	--	0.127
c	0.46	0.50	0.60
c2	0.46	0.50	0.58
D1	5.21	--	--
E1	4.40	--	--
θ	0°	--	10°

Figure 19. TO252-3L Package outline

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