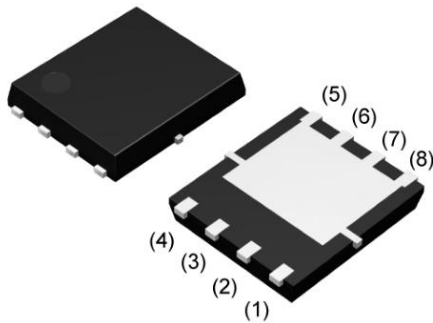


**Description**
**40V N-CHANNEL ENHANCEMENT MODE POWER MOSFET**
**Features**

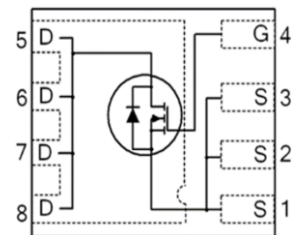
- Device Rating  $V_{DS} = 40V$ ,  $I_D = 195A$
- $R_{DS(ON)} = 1.45m\Omega$  (typ.) @  $V_{GS} = 10V$ ,  $I_D = 40A$
- Proprietary High Density Trench Technology
- RoHS Compliant & Halogen-Free

**Application**

- Battery Management System
- Load Switch
- Brushless DC Motor Control

**Package**


**DFN5\*6**  
**JFG195N40L**


**Absolute Maximum Ratings**  $T_C = 25^\circ C$  unless otherwise specified

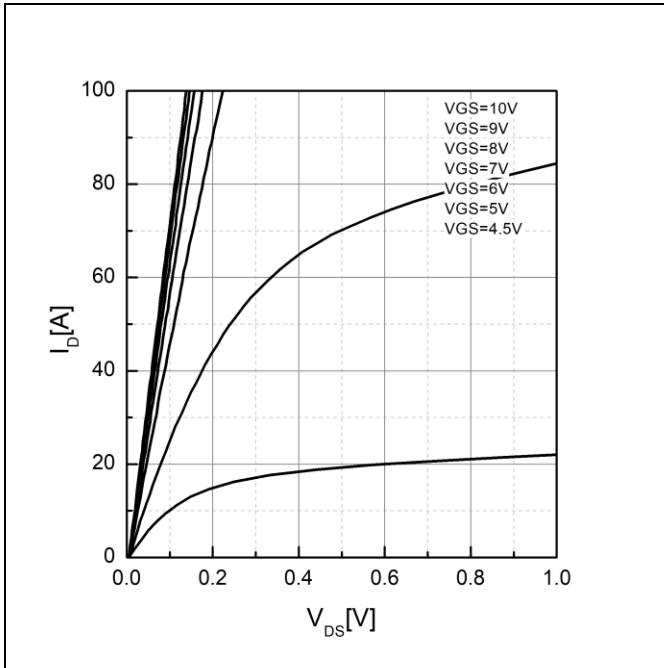
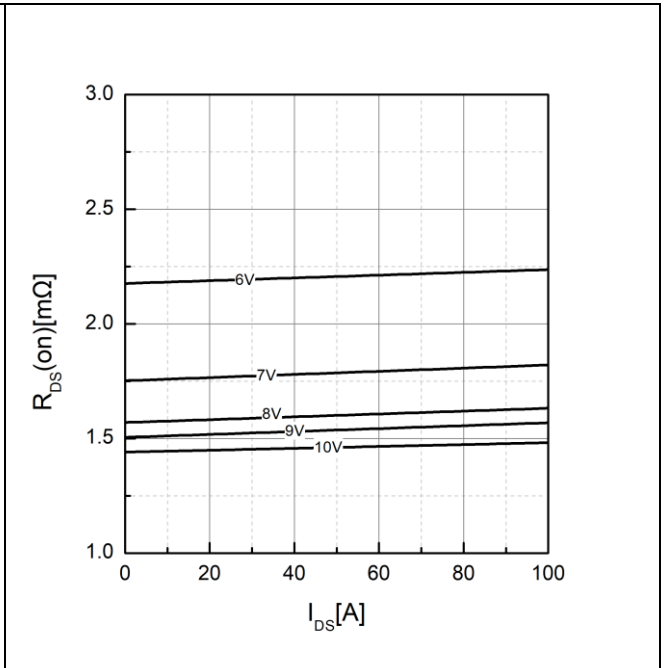
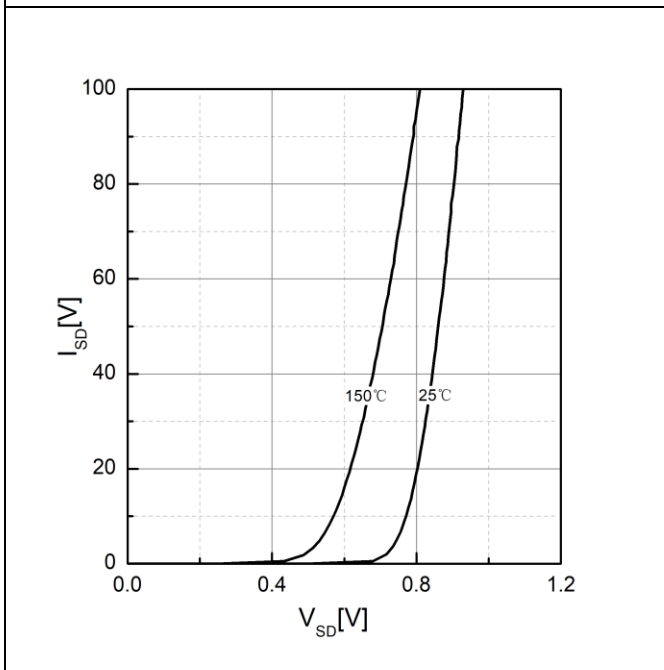
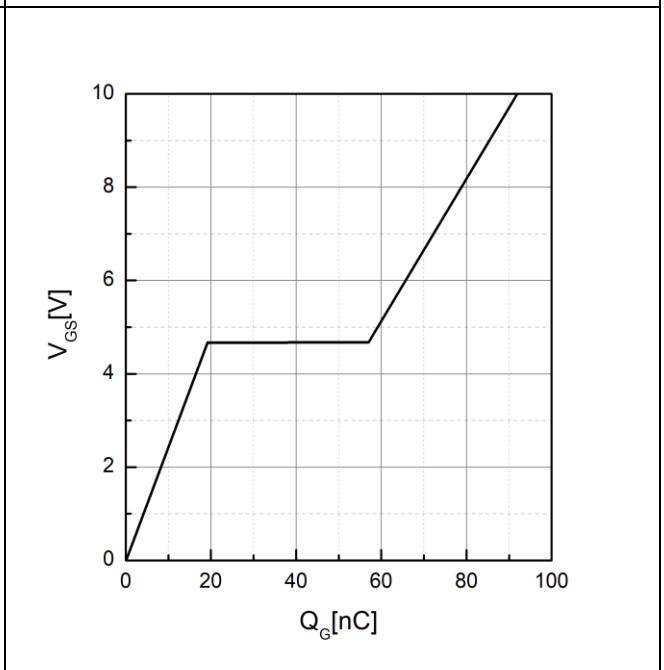
Symbol	Parameter	Max.	Units	
$V_{DS}$	Drain-Source Voltage	40	V	
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V	
$I_D$	Continuous Drain Current, $V_{GS} @ 10V$ <sup>note1</sup>	$T_C = 25^\circ C$	195	A
		$T_C = 100^\circ C$	123	A
$I_{DM}$	Pulsed Drain Current <sup>note2</sup>	780	A	
$P_D$	Power Dissipation <sup>note4</sup>	$T_C = 25^\circ C$	100	W
	Power Dissipation	$T_A = 25^\circ C$	2.6	W
$E_{AS}$	Single Pulsed Avalanche Energy <sup>note3</sup>	273	mJ	
$R_{\theta JC}$	Thermal Resistance, Junction to Case <sup>note1</sup>	1.24	$^\circ C/W$	
$R_{\theta JA}$	Junction-to-Ambient (mounted on 1 inch square PCB)	48	$^\circ C/W$	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$	

**Electrical Characteristics**  $T_C=25^{\circ}\text{C}$  unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 1mA$	40	-	-	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS} = 40V, V_{GS} = 0V$	-	-	1	$\mu A$
$I_{GSS}$	Gate-Source Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$	-100	-	100	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2	-	4	V
$R_{DS(on)}$	Static Drain-Source On-Resistance <sup>note2</sup>	$V_{GS} = 10V, I_D = 40A$	-	1.45	1.7	m $\Omega$
		$V_{GS} = 6V, I_D = 40A$	-	2.90	-	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 5V, I_D = 40A$	-	298	-	S
<b>Dynamic Characteristics</b>						
$R_g$	Gate Resistance		-	0.8	-	$\Omega$
$C_{iss}$	Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1MHz$	-	4100	-	pF
$C_{oss}$	Output Capacitance		-	775	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	715	-	pF
$Q_g$	Total Gate Charge	$V_{DS} = 20V, I_D = 40A,$ $V_{GS} = 10V$	-	92	-	nC
$Q_{gs}$	Gate-Source Charge		-	19.2	-	nC
$Q_{gd}$	Gate-Drain("Miller") Charge		-	37.8	-	nC
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20V, I_D = 40A,$ $R_G = 1\Omega, V_{GS} = 10V$	-	106	-	ns
$t_r$	Turn-On Rise Time		-	110	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	128	-	ns
$t_f$	Turn-Off Fall Time		-	88	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Diode Forward Current <sup>note1,5</sup>		-	160	-	A
$I_{SM}$	Maximum Pulsed Diode Forward Current <sup>note2,5</sup>		-	780	-	A
$t_{rr}$	Reverse Recovery Time	$T_J = 25^{\circ}\text{C}, I_F = 40A$ $di/dt = 125A/\mu s$	-	41	-	ns
$Q_{rr}$	Reverse Recovery Charge	$T_J = 25^{\circ}\text{C}, I_F = 40A$ $di/dt = 125A/\mu s$	-	67	-	nC
$V_{SD}$ <sup>note2</sup>	Drain to Source Diode Forward Voltage	$T_J = 25^{\circ}\text{C}, I_S = 40A,$ $V_{GS} = 0V$	-	0.81	-	V

Note :

- 1.The data tested by surface mounted on one inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed, pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .
- 3.The EAS data shows Max. rating. The test condition is  $V_{DD}=25V, V_{GS}=10V, R_g=25\Omega, L=0.1mH, I_{AS}=73.8A$ .
- 4.The power dissipation is limited by  $150^{\circ}\text{C}$  junction temperature.
- 5.The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.

**Typical Performance Characteristics**

**Figure 1. Output Characteristics TJ=25°C**

**Figure 2. Drain-source on resistance TJ=25°C**

**Figure 3. Forward characteristics of body diode**

**Figure 4. Gate Charge Characteristics**

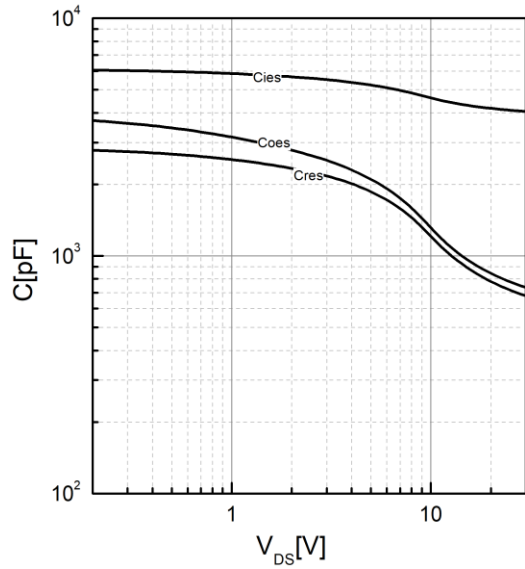


Figure 5. Capacitance Characteristics

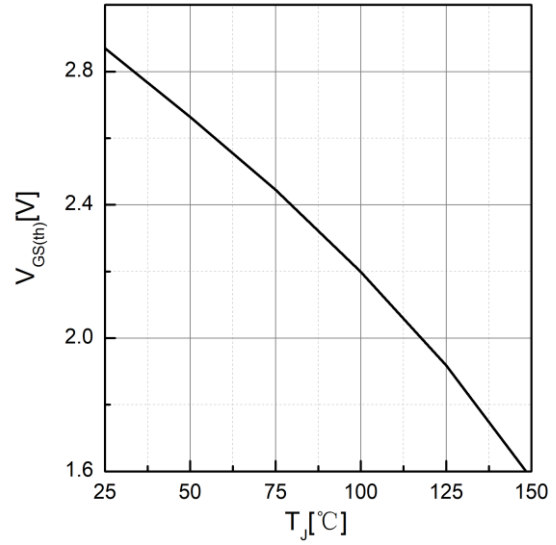


Figure 6. Threshold Voltage Vs. Temperature

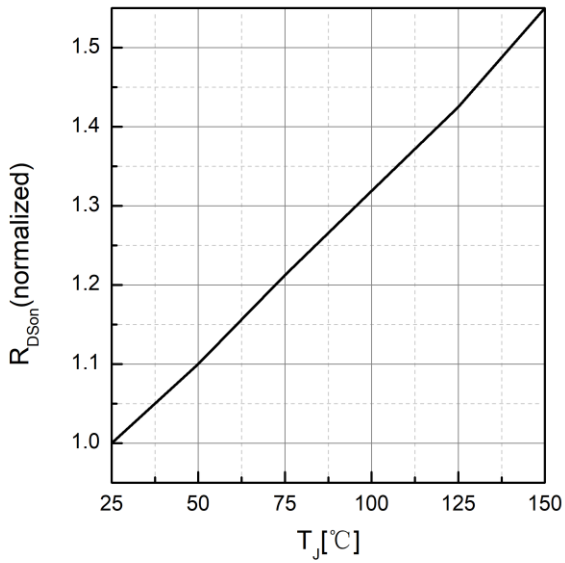


Figure 7. Drain-source on-state resistance

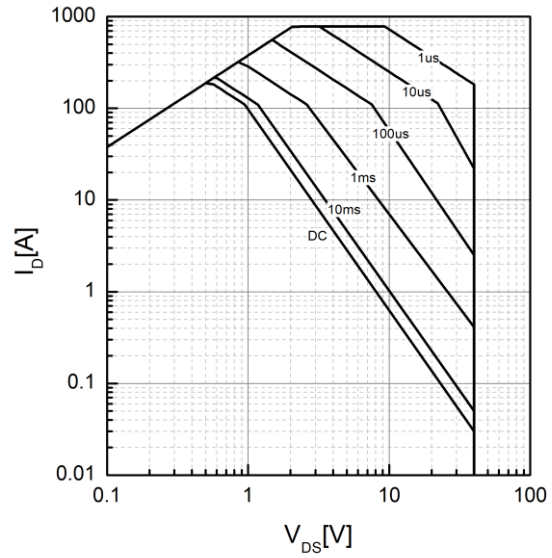


Figure 8. Maximum Safe Operating Area

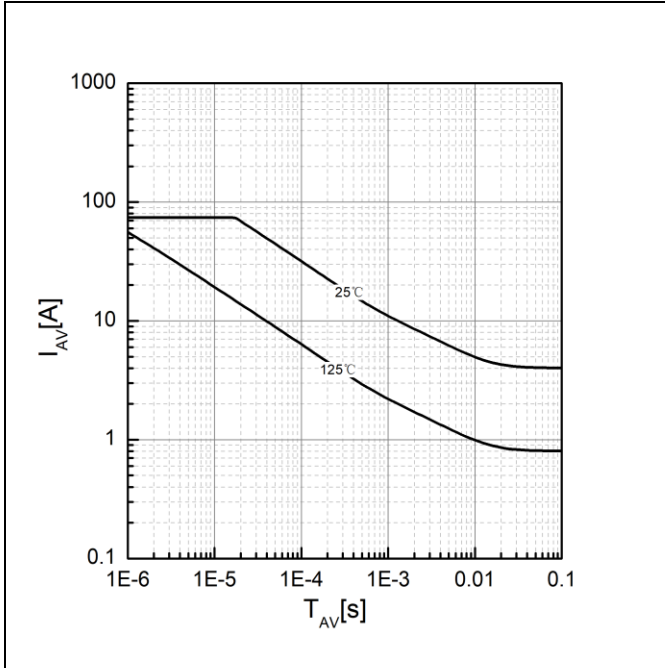


Figure 9. Avalanche characteristics

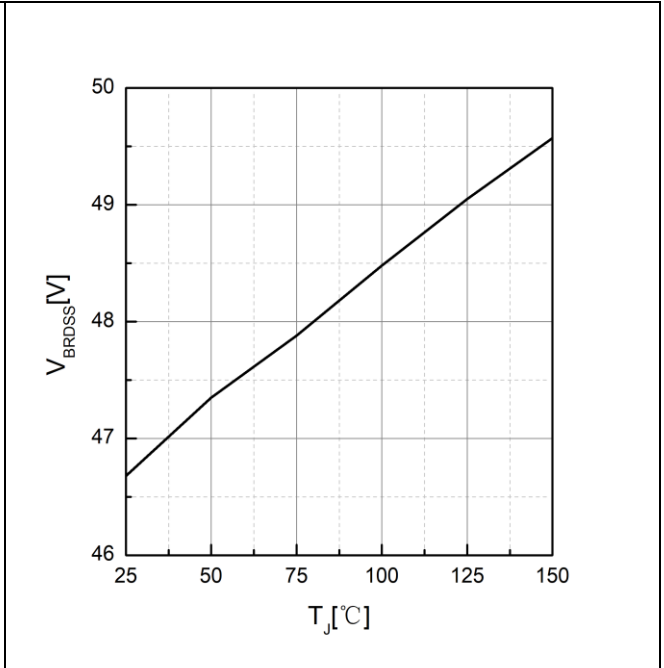


Figure 10. Drain-source breakdown voltage

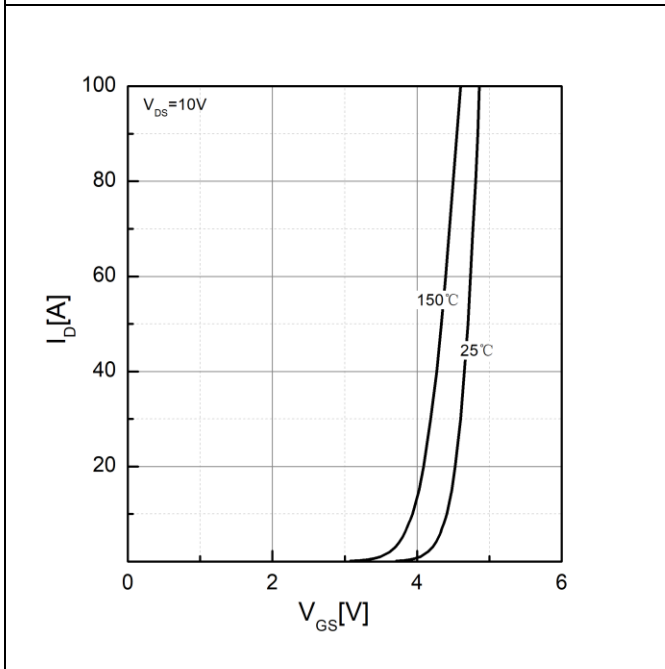


Figure 11. Transfer characteristics

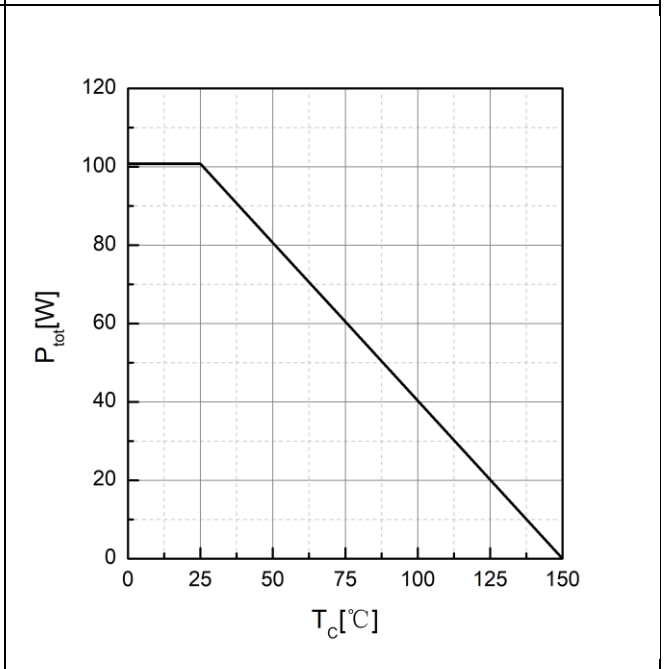


Figure 12. Power dissipation

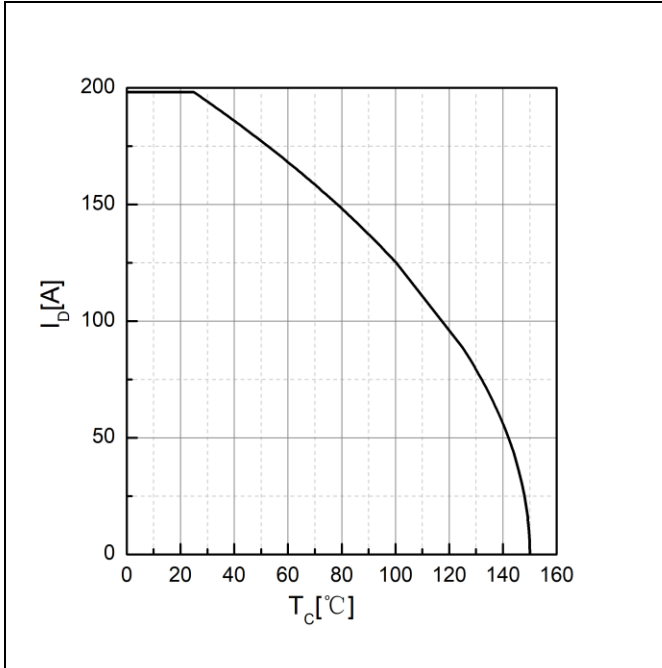


Figure 13. Drain current

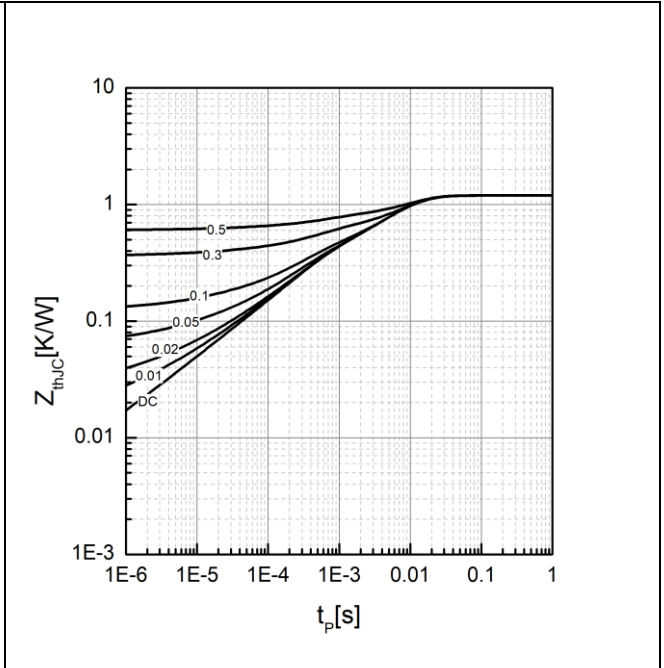


Figure 14. Effective Transient Thermal Impedance

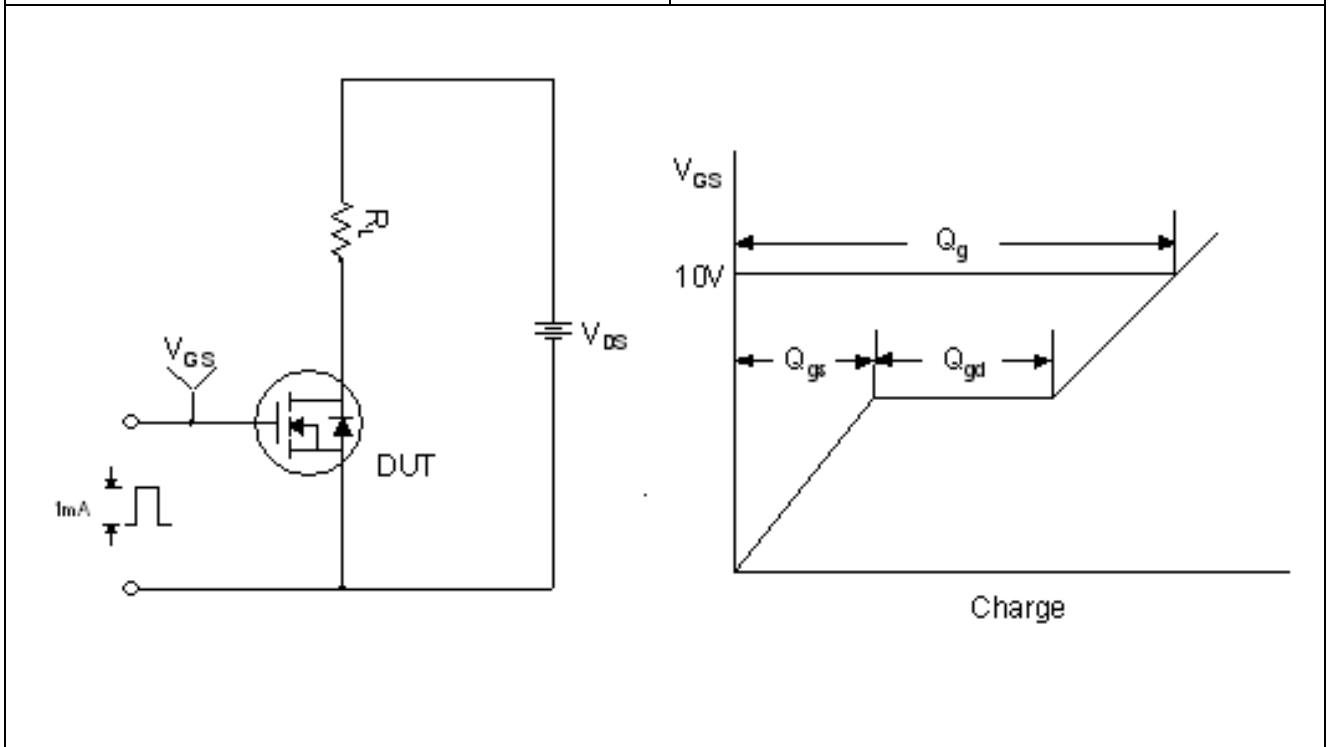


Figure 15. Gate Charge Test Circuit & Waveform

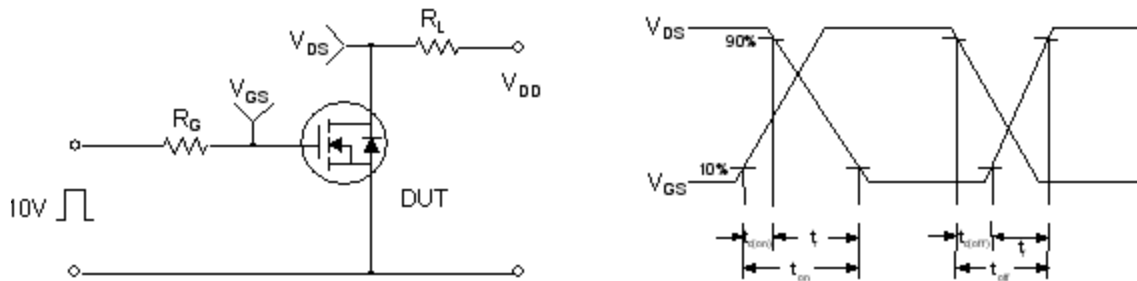


Figure 16. Resistive Switching Test Circuit & Waveforms

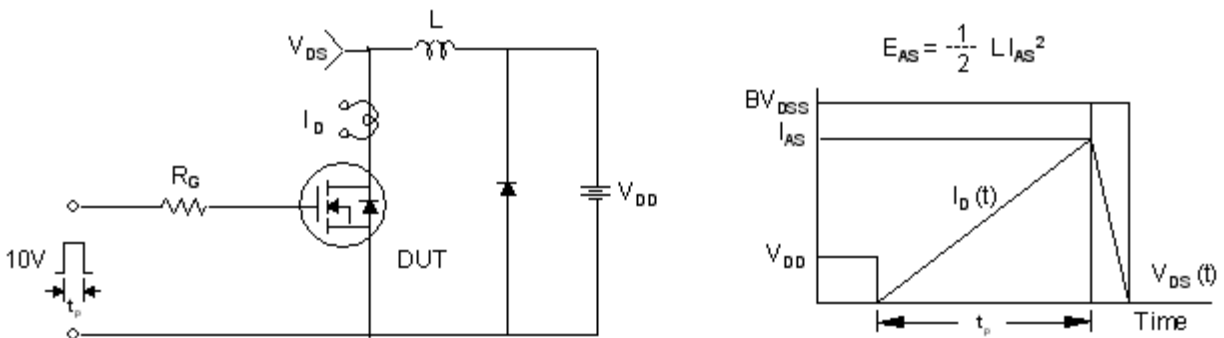
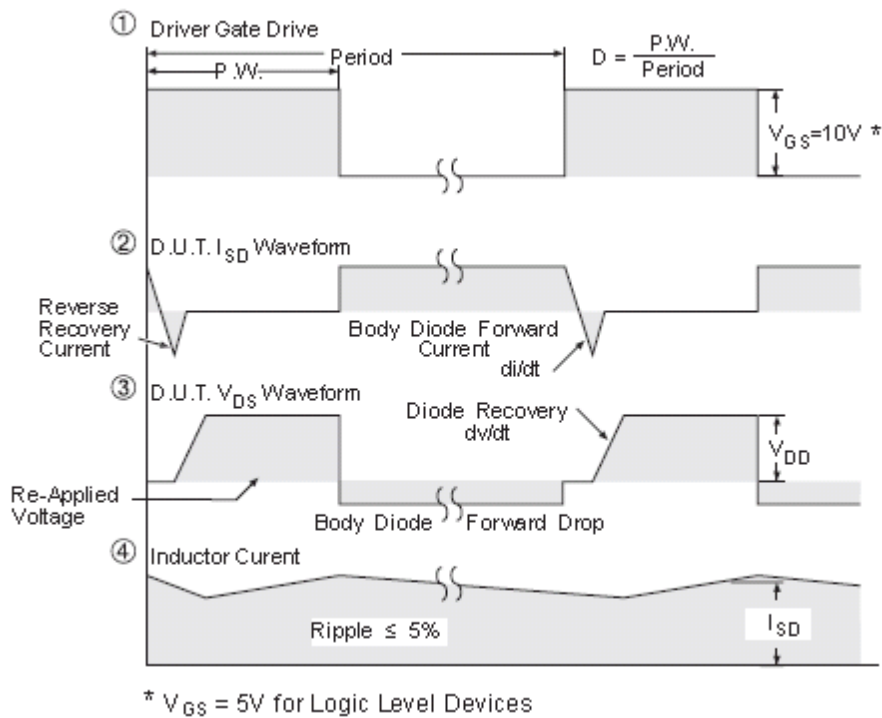
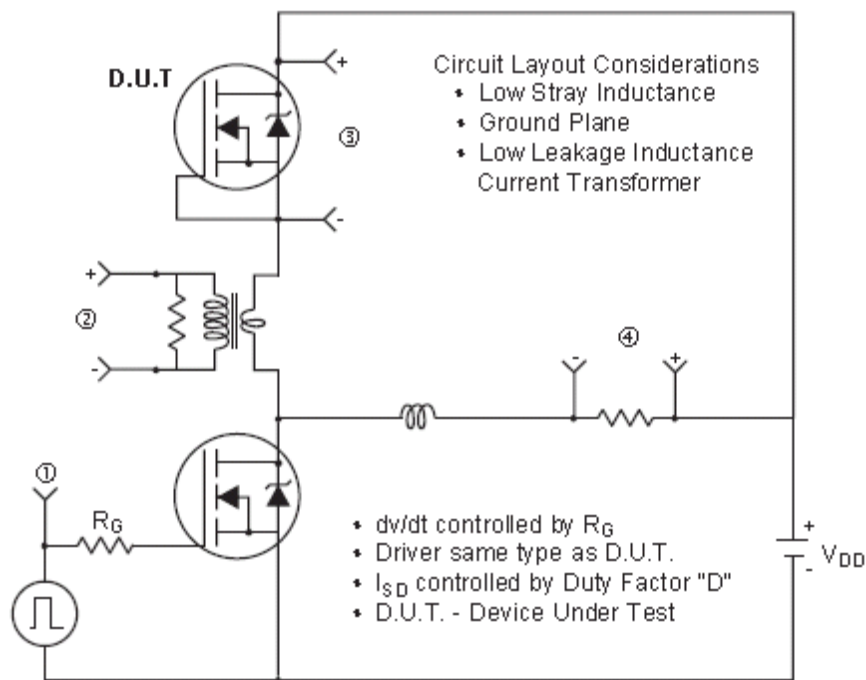
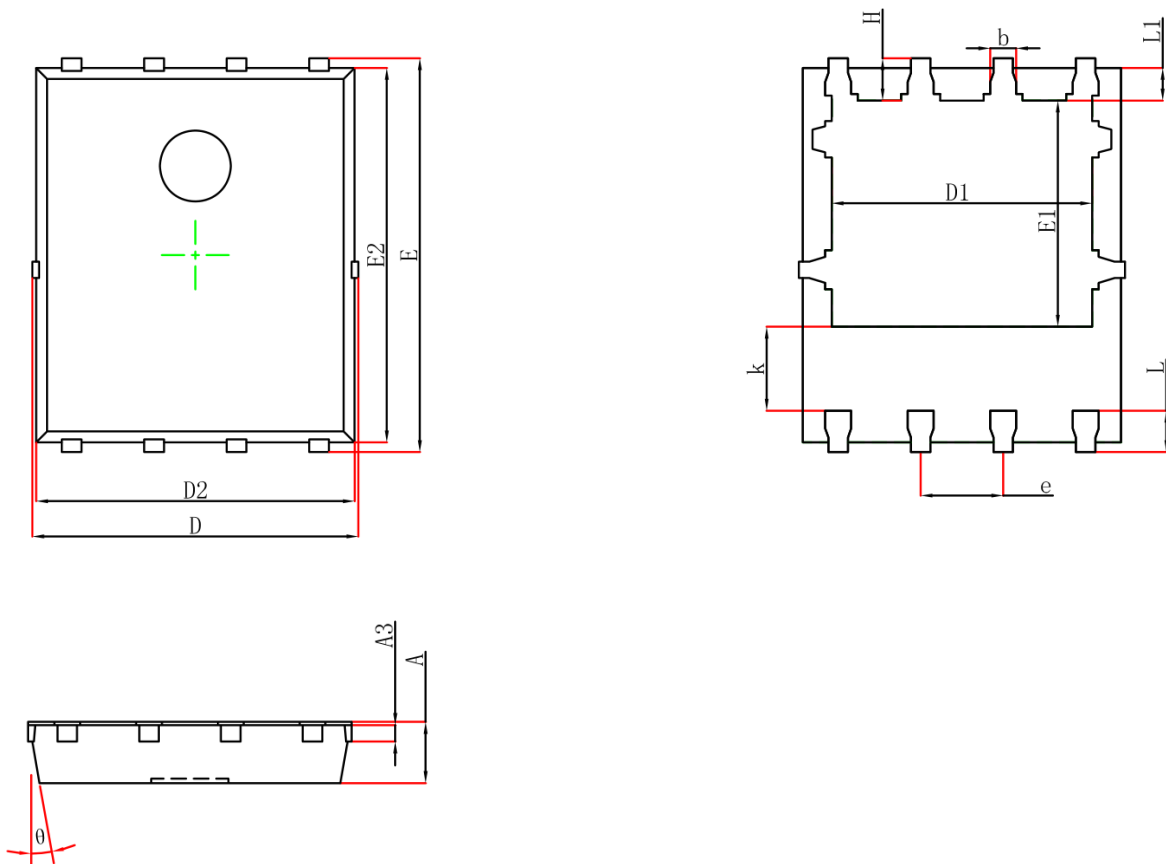


Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms



**Figure 18. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms (For N-channel)**



**Package outline**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF		0.010REF	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP		0.050TYP	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
$\theta$	10°	12°	10°	12°

**Figure 19. DFN 5x6 Package outline**

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