Description

30V N-CHANNEL ENHANCEMENT MODE POWER MOSFET

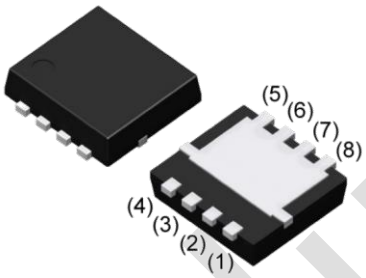
Features

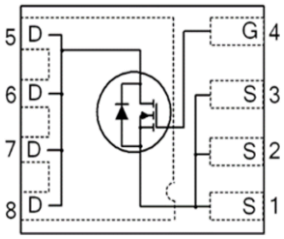
- Device Rating V_{DS} = 30V, I_D = 182A
- $R_{DS(ON)}$ =2.1mΩ (typ.) @ V_{GS} = 10V, I_D = 30A
- SGT Technology
- 100% avalanche test
- Qualified according to JEDEC for target applications
- RoHS Compliant & Halogen-Free

Application

- DC-DC converters for server and telecommunications
- Power delivery for V-core, ASIC, DDR, GPU, VGA and system components
- Point-of-Load (POL) modules
- Secondary-side synchronous rectification
- Voltage regulator modules (VRM)
- Brushed and brushless motor control

Package





DFN 3.3*3.3-8L

JFG182N30K

Absolute Maximum Ratings T_C=25℃ unless otherwise specified

Symbol	Parameter		Max.	Units
V_{DS}	Drain-Source Voltage		30	V
V_{GS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current, VGS @ 10V note1	T_C = 25℃	182	A
		T_C = 100℃	115	A
I_{DM}	Pulsed Drain Current note2		308	A
P_D	Power Dissipation note4	T_C = 25℃	125	W
	Power Dissipation	T_A = 25℃	2.08	W
E_{AS}	Single Pulsed Avalanche Energy note3		103	mJ
$R_{\theta JC}$	Thermal Resistance, Junction to Case note1		1.0	℃/W
$R_{\theta JA}$	Junction to Ambient (mounted on 1 inch square PCB)		60	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

Electrical Characteristics T_C=25℃ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	30	-	-	V
I_{DSS}	Drain-Source Leakage Current	V_{DS}=30V,V_{GS}= 0V, T_C = 25℃	-	-	1	μA
		V_{DS}=30V,V_{GS}= 0V, T_C = 55℃	-	-	10	μA
I_{GSS}	Gate-Source Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-100	-	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1	-	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance note2	V_{GS} = 10V, I_D =30A	-	2.1	2.6	mΩ
$R_{DS(on)}$	Static Drain-Source On-Resistance note2	V_{GS} = 4.5V, I_D =30A	-	2.8	3.4	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 1V, I_D =30A	-	108	-	S
Dynamic Characteristics						
R_g	Gate Resistance		-	3.1	-	Ω
C_{iss}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz	-	1780	-	pF
C_{oss}	Output Capacitance		-	560	-	pF
C_{rss}	Reverse Transfer Capacitance		-	40	-	pF
Q_g	Total Gate Charge	V_{DS} =15V, I_D = 30A, V_{GS} = 10V	-	25	-	nC
Q_{gs}	Gate-Source Charge		-	6.0	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	3.7	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15V, I_D = 30A, R_G = 1Ω, V_{GS} = 10V	-	10	-	ns
t_r	Turn-On Rise Time		-	15	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	25	-	ns
t_f	Turn-Off Fall Time		-	6	-	ns
Source-Drain Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Diode Forward Current note1,5		-	-	83	A
I_{SM}	Maximum Pulsed Diode Forward Current note2,5		-	-	308	A
t_{rr}	Reverse Recovery Time	T_J = 25°C, I_S = 30A, V_{GS} = 0V di/dt = 200A/μs	-	32	-	ns
Q_{rr}	Reverse Recovery Charge		-	19	-	nC
V_{SD} note2	Source to Drain Diode Forward Voltage	T_J = 25°C, I_S = 30A, V_{GS} = 0V	-	0.81	-	V

Note :

1.The data tested by surface mounted on one $inch^2$ FR-4 board with 2OZ copper.

2.The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.

3.The EAS data shows Max. rating. The test condition is L=0.1mH, IAS= 48 A.

4.The power dissipation is limited by 150℃ junction temperature.

5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Performance Characteristics

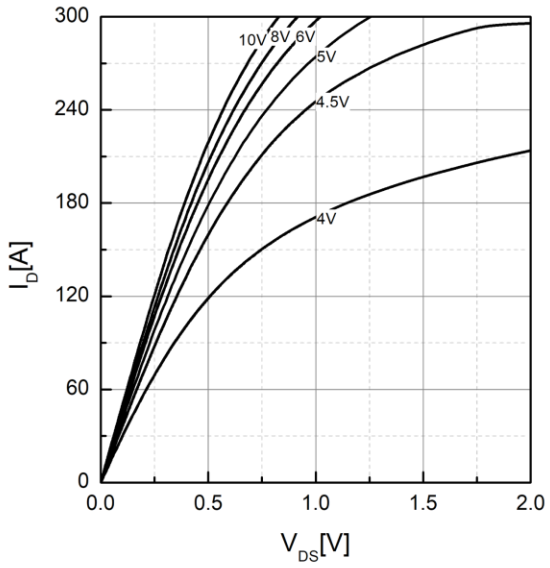


Figure 1. Output Characteristics, TJ=25℃

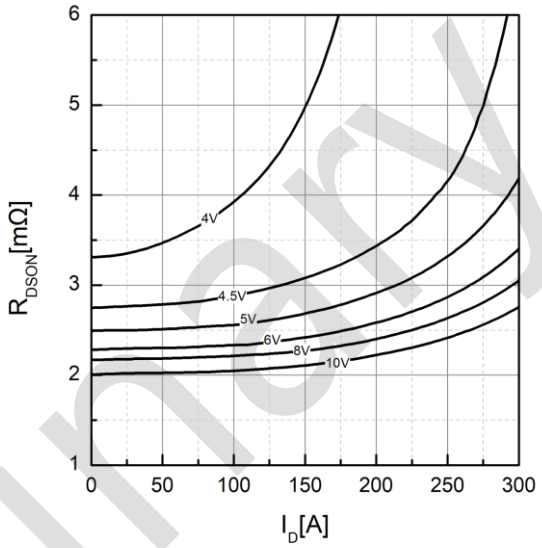


Figure 2. Drain-source on resistance , TJ=25℃

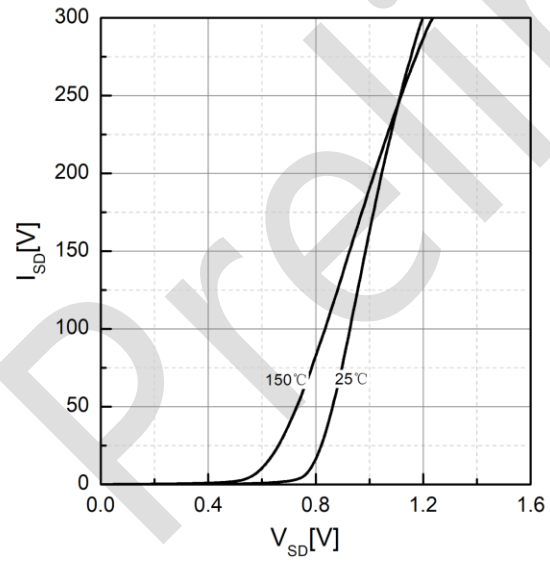


Figure 3. Forward characteristics of body diode

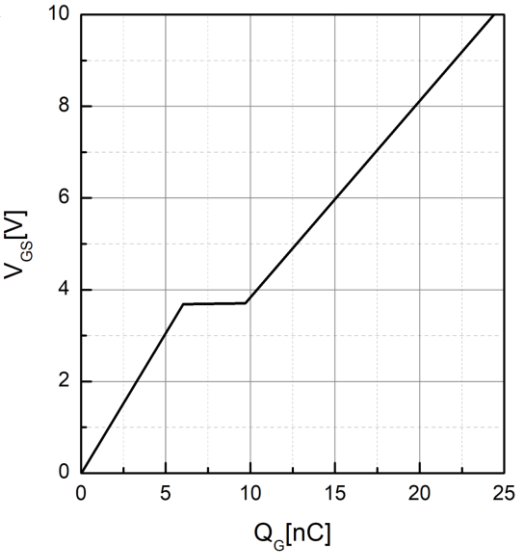


Figure 4. Gate Charge Characteristics

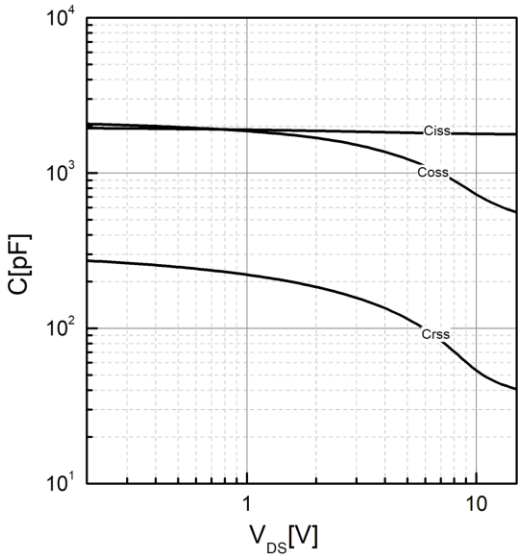


Figure 5. Capacitance Characteristics

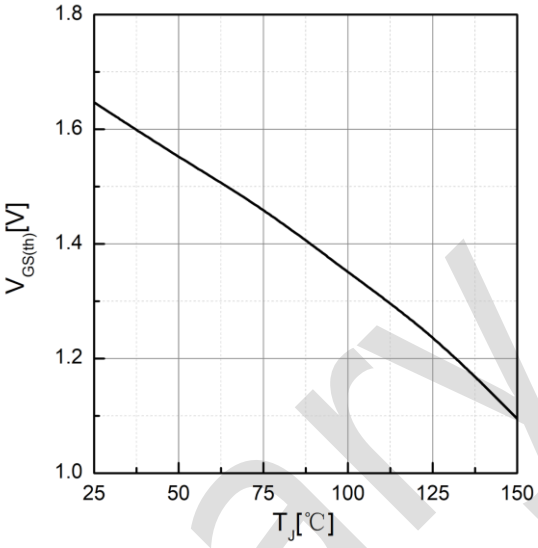


Figure 6. Threshold Voltage Vs. Temperature

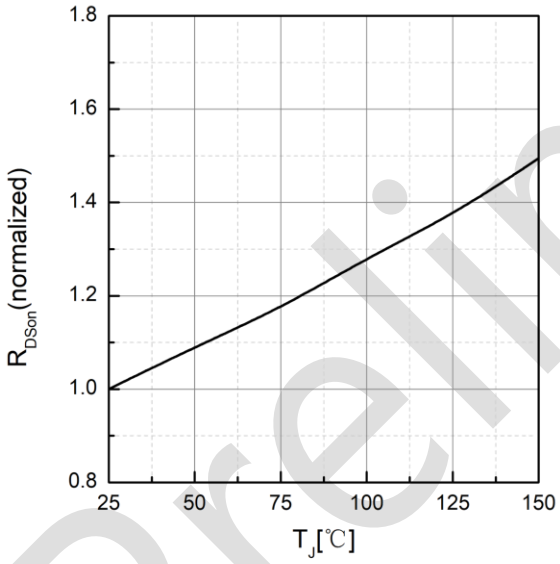


Figure 7. Drain-source on-state resistance

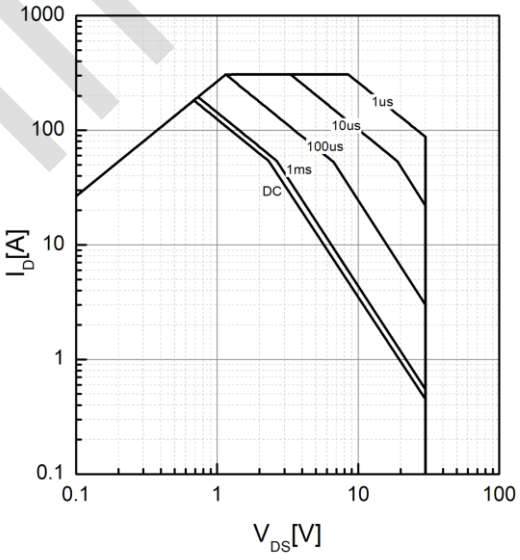


Figure 8. Maximum Safe Operating Area

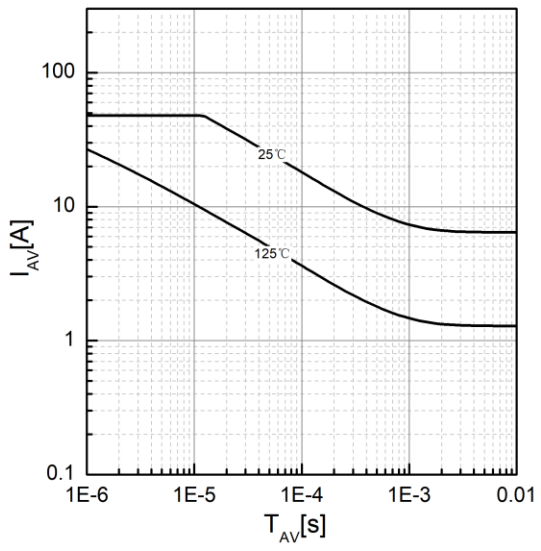


Figure 9. Avalanche characteristics

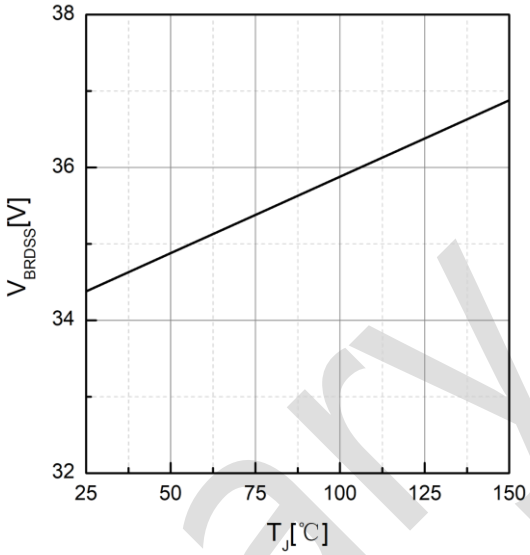


Figure 10. Drain-source breakdown voltage

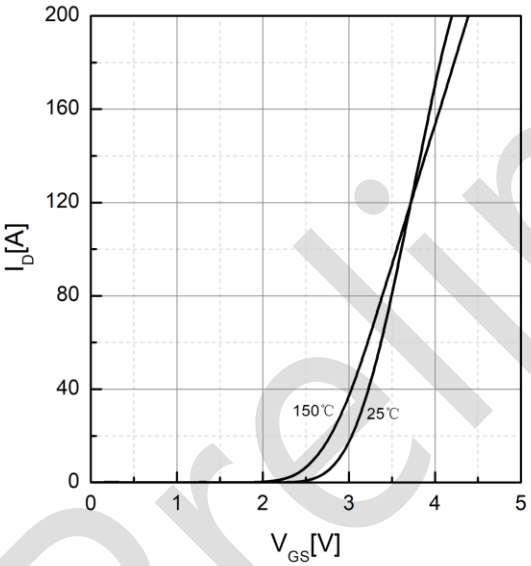


Figure 11. Transfer characteristics

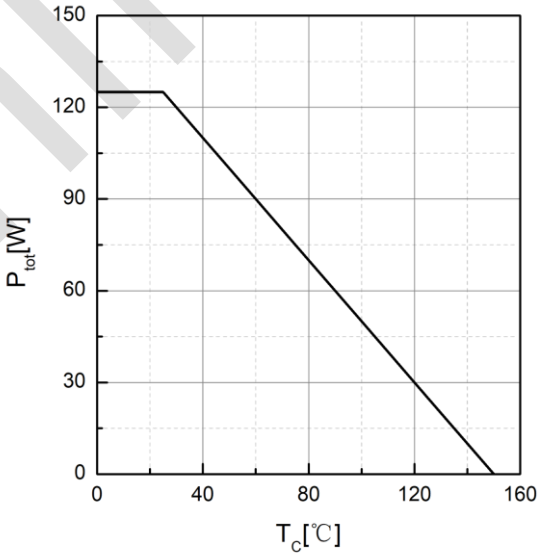


Figure 12. Power dissipation

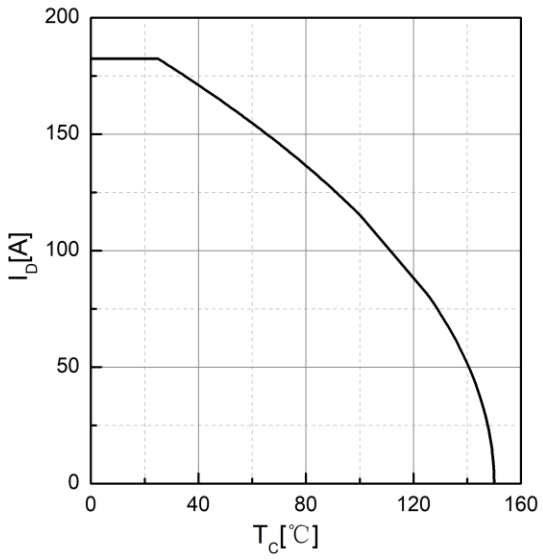


Figure 13. Drain current

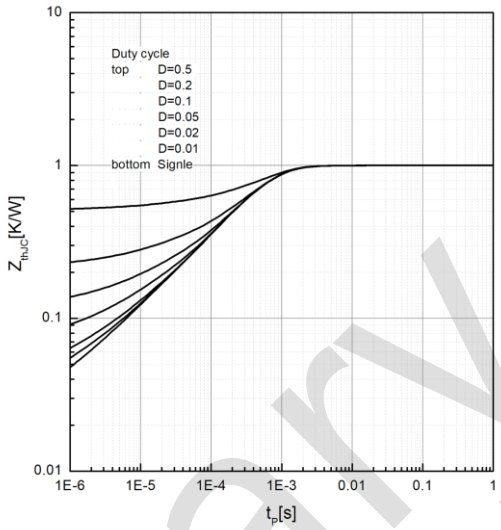


Figure 14. Effective Transient Thermal Impedance

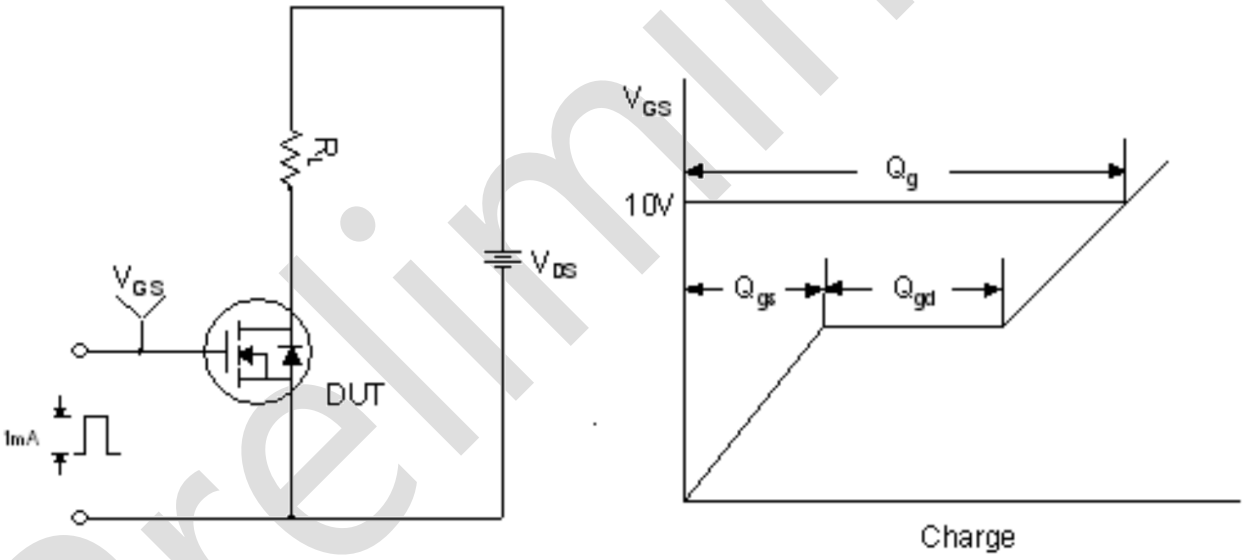


Figure 15. Gate Charge Test Circuit & Waveform

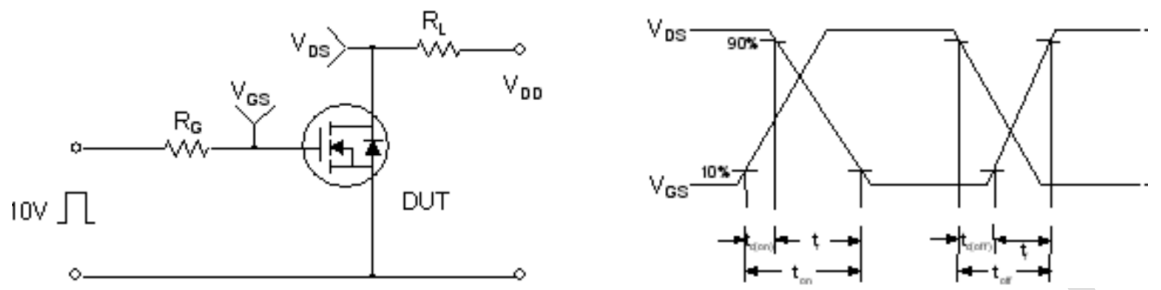


Figure 16. Resistive Switching Test Circuit & Waveforms

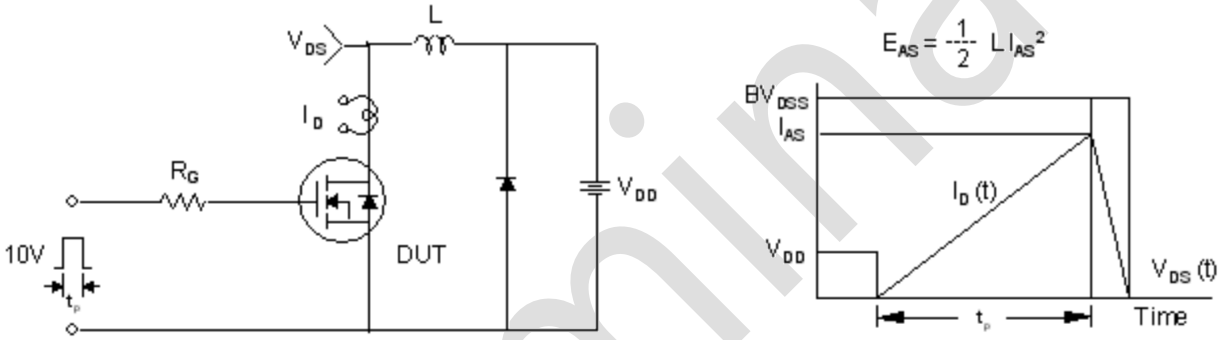


Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms

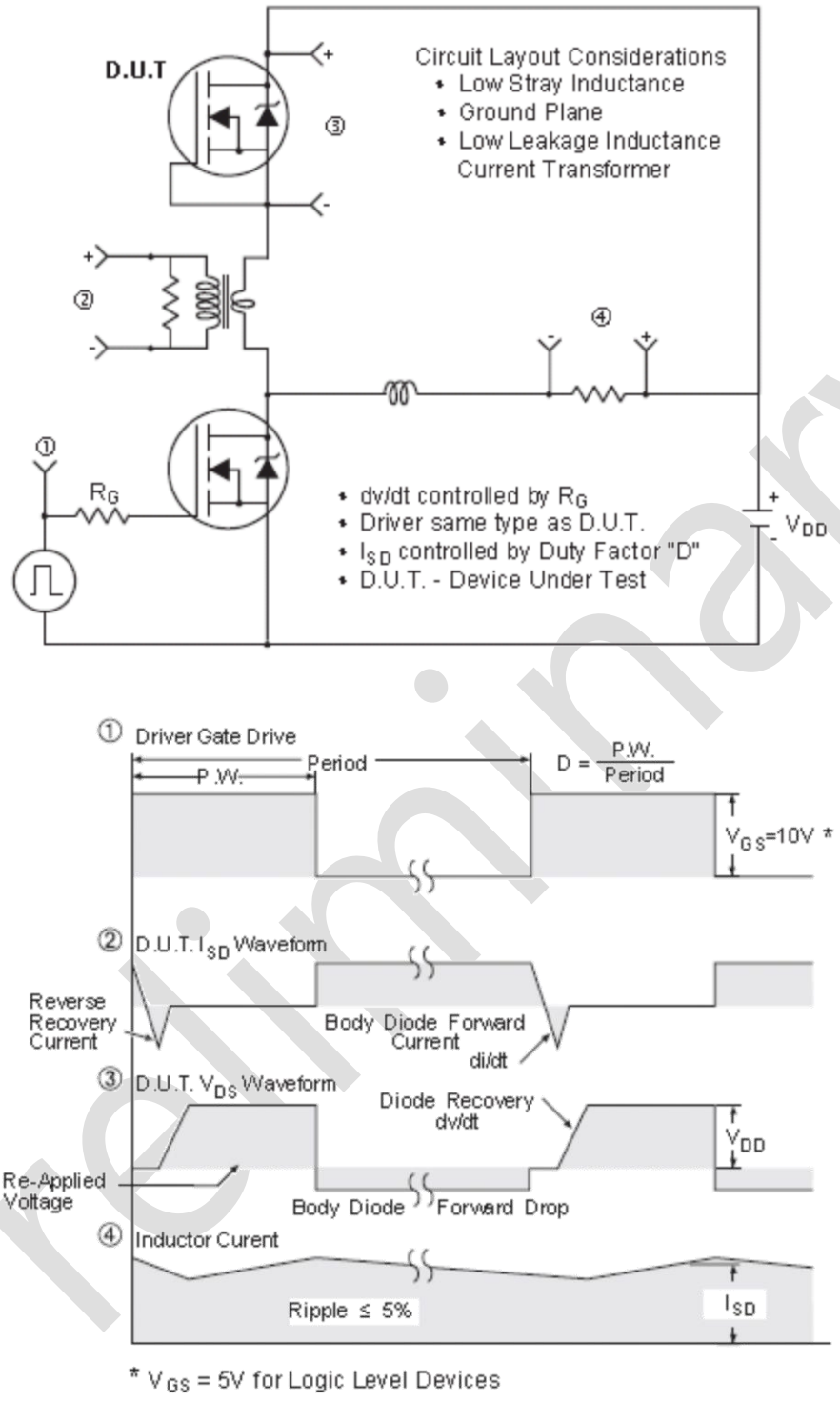
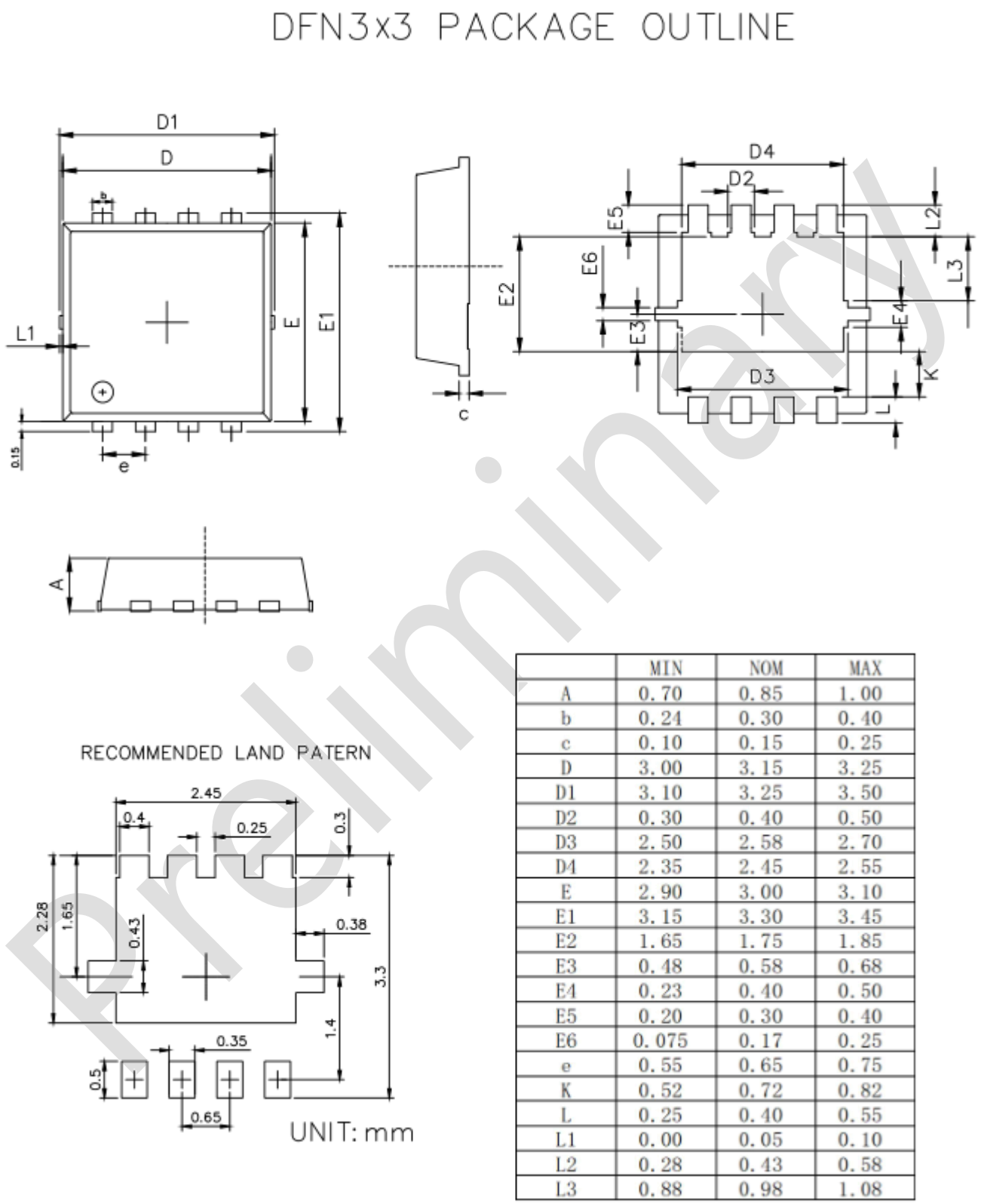


Figure 18. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

Package outline



	MIN	NOM	MAX
A	0.70	0.85	1.00
b	0.24	0.30	0.40
c	0.10	0.15	0.25
D	3.00	3.15	3.25
D1	3.10	3.25	3.50
D2	0.30	0.40	0.50
D3	2.50	2.58	2.70
D4	2.35	2.45	2.55
E	2.90	3.00	3.10
E1	3.15	3.30	3.45
E2	1.65	1.75	1.85
E3	0.48	0.58	0.68
E4	0.23	0.40	0.50
E5	0.20	0.30	0.40
E6	0.075	0.17	0.25
e	0.55	0.65	0.75
K	0.52	0.72	0.82
L	0.25	0.40	0.55
L1	0.00	0.05	0.10
L2	0.28	0.43	0.58
L3	0.88	0.98	1.08

Figure 19. DFN 3.3x3.3 Package outline

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