Description

100V N-CHANNEL ENHANCEMENT MODE POWER MOSFET

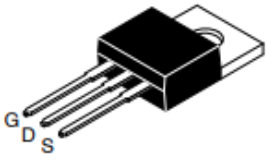
Features

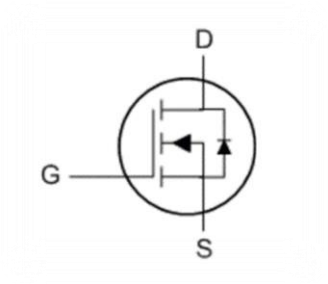
- Device Rating V_{DS} = 100V, I_D = 166A
- $R_{DS(ON)}$ =4.6mΩ (typ.) @ V_{GS} = 10V, I_D = 50A
- Proprietary High Density Trench Technology
- RoHS Compliant & Halogen-Free

Application

- Battery management
- System and Power managerment

Package





TO-220-3L

JFG166N100B

Absolute Maximum Ratings T_C=25℃ unless otherwise specified

Symbol	Parameter		Max. TO-220-3L	Units
V_{DS}	Drain-Source Voltage		100	V
V_{GS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current, VGS @ 10V note1	T_C = 25℃	166	A
		T_C = 100℃	105	A
I_{DM}	Pulsed Drain Current note2		664	A
P_D	Power Dissipation note4	T_C = 25℃	277	W
	Power Dissipation	T_A = 25℃	3.12	W
E_{AS}	Single Pulsed Avalanche Energy note3		729	mJ
$R_{\theta JC}$	Thermal Resistance, Junction to Case note1		0.45	℃/W
$R_{\theta JA}$	Junction to Ambient (mounted on 1 inch square PCB)		40	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

Electrical Characteristics T_C=25℃ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	100	-	-	V
I_{DSS}	Drain-Source Leakage Current	V_{DS}=100V,V_{GS}= 0V, T_C = 25℃	-	-	1	μA
		V_{DS}=100V,V_{GS}= 0V, T_C = 55℃	-	-	10	μA
I_{GSS}	Gate-Source Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-100	-	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	2	-	4	V
$R_{DS(on)}$	Static Drain-Source On-Resistance note2	V_{GS} = 10V, I_D =50A	-	4.6	5.5	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 5V, I_D =50A	-	91	-	S
Dynamic Characteristics						
R_g	Gate Resistance		-	0.3	-	Ω
C_{iss}	Input Capacitance	V_{DS} = 50V, V_{GS} = 0V, f = 1MHz	-	2990	-	pF
C_{oss}	Output Capacitance		-	572	-	pF
C_{rss}	Reverse Transfer Capacitance		-	41	-	pF
Q_g	Total Gate Charge	V_{DS} =50V, I_D = 50A, V_{GS} = 10V	-	51	-	nC
Q_{gs}	Gate-Source Charge		-	14	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	16	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50V, I_D = 50A, R_G = 1Ω, V_{GS} = 10V	-	26	-	ns
t_r	Turn-On Rise Time		-	28	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	33	-	ns
t_f	Turn-Off Fall Time		-	10	-	ns
Source-Drain Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Diode Forward Current note1,5		-	-	230	A
I_{SM}	Maximum Pulsed Diode Forward Current note2,5		-	-	664	A
t_{rr}	Reverse Recovery Time	T_J = 25°C, I_S = 50A, V_{GS} = 0V di/dt = 100A/μs	-	500	-	ns
Q_{rr}	Reverse Recovery Charge		-	100	-	nC
V_{SD} note2	Source to Drain Diode Forward Voltage	T_J = 25°C, I_S = 50A, V_{GS} = 0V	-	0.90	-	V

Note :

1.The data tested by surface mounted on one $inch^2$ FR-4 board with 2OZ copper.

2.The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.

3.The EAS data shows Max. rating. The test condition is L=0.5mH, IAS= 54A.

4.The power dissipation is limited by 150℃ junction temperature.

5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Performance Characteristics

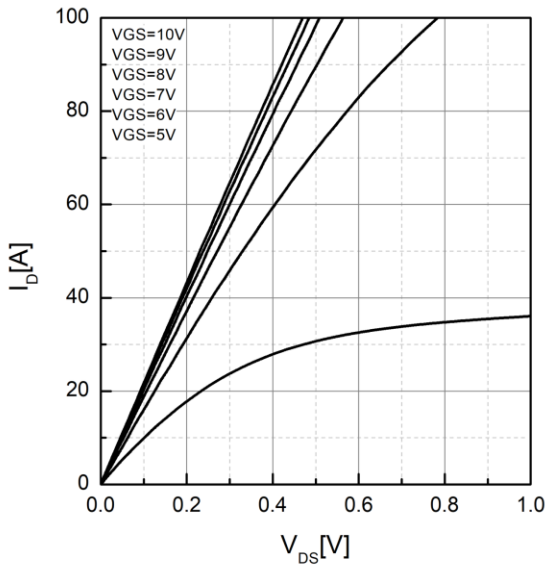


Figure 1. Output Characteristics, TJ=25℃

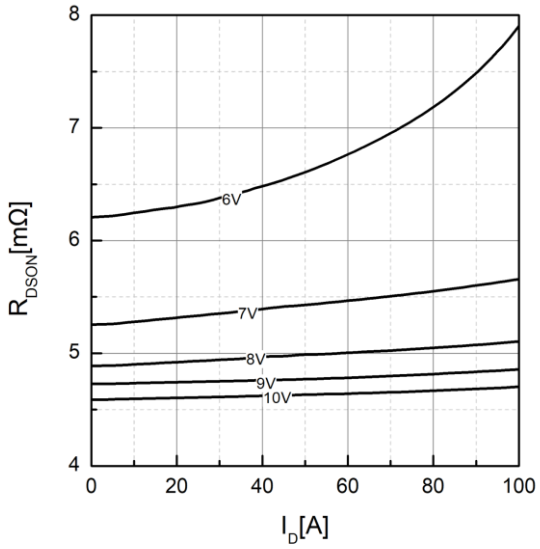


Figure 2. Drain-source on resistance , TJ=25℃

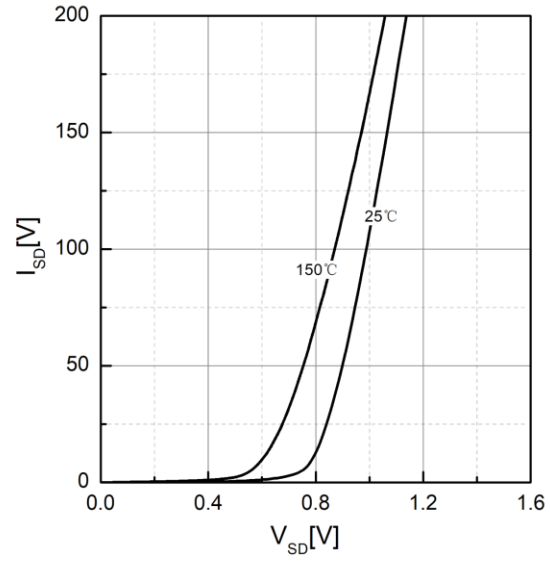


Figure 3. Forward characteristics of body diode

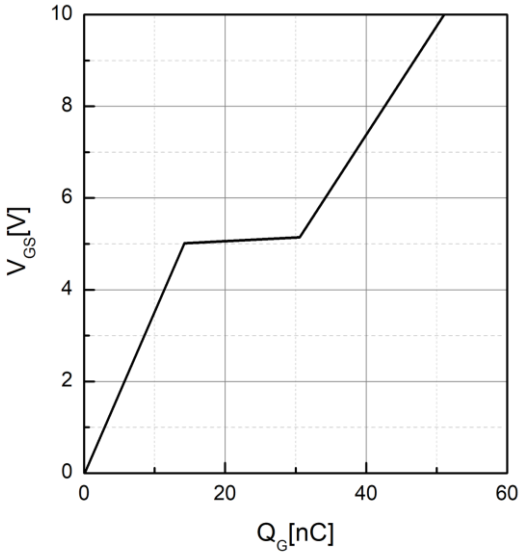


Figure 4. Gate Charge Characteristics

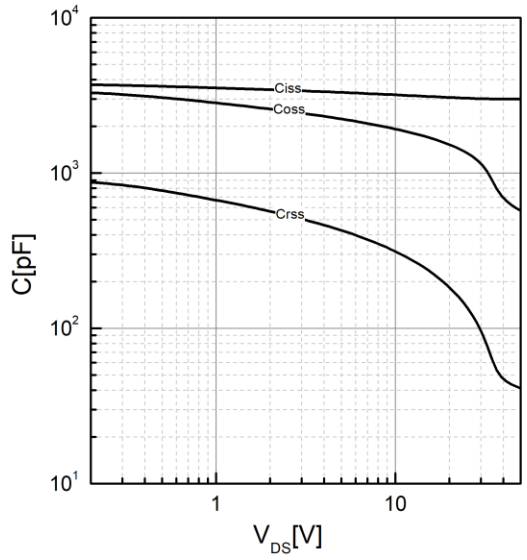


Figure 5. Capacitance Characteristics

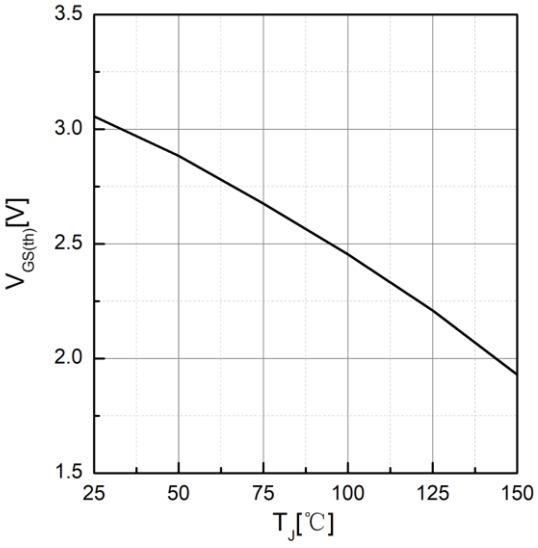


Figure 6. Threshold Voltage Vs. Temperature

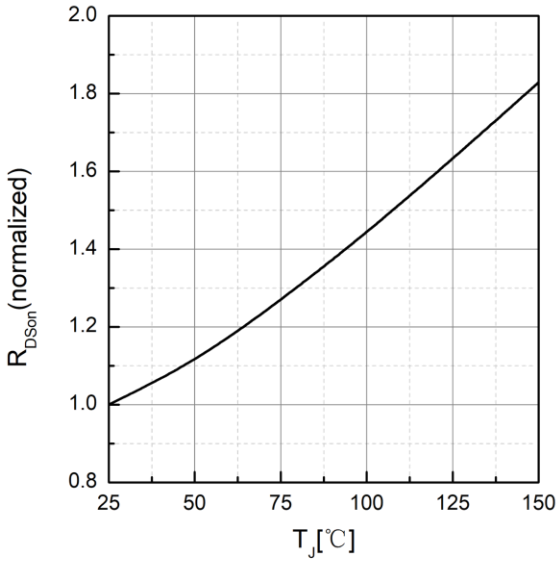


Figure 7. Drain-source on-state resistance

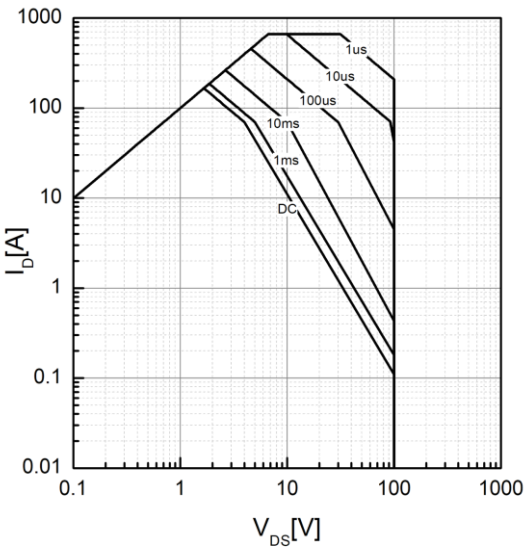


Figure 8. Maximum Safe Operating Area

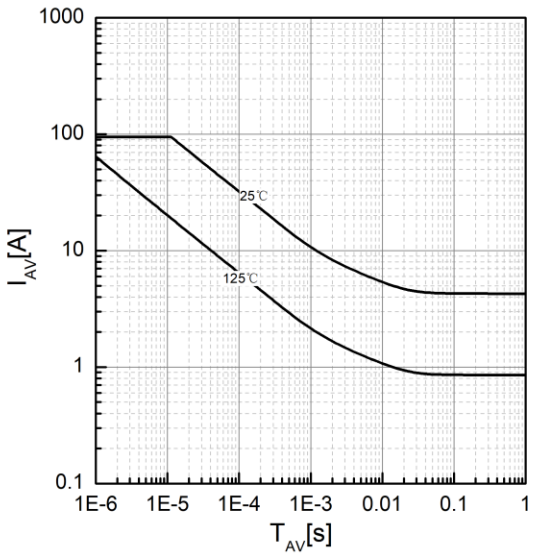


Figure 9. Avalanche characteristics

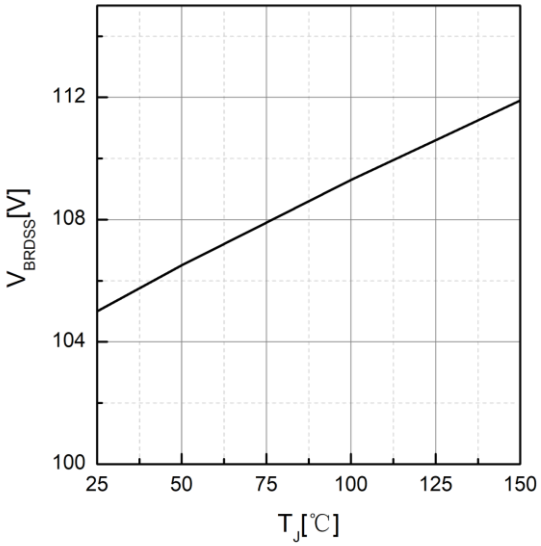


Figure 10. Drain-source breakdown voltage

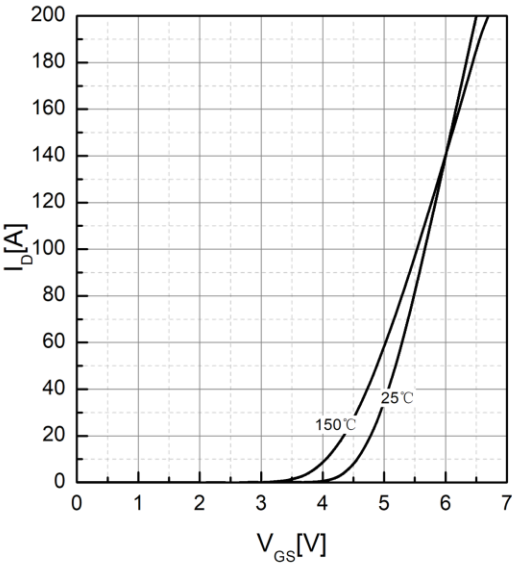


Figure 11. Transfer characteristics

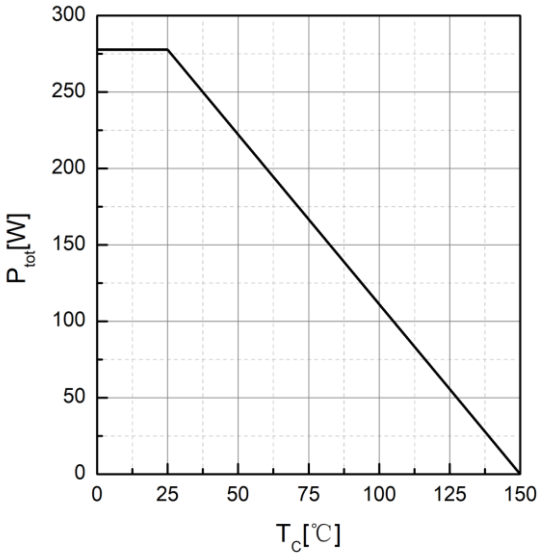


Figure 12. Power dissipation

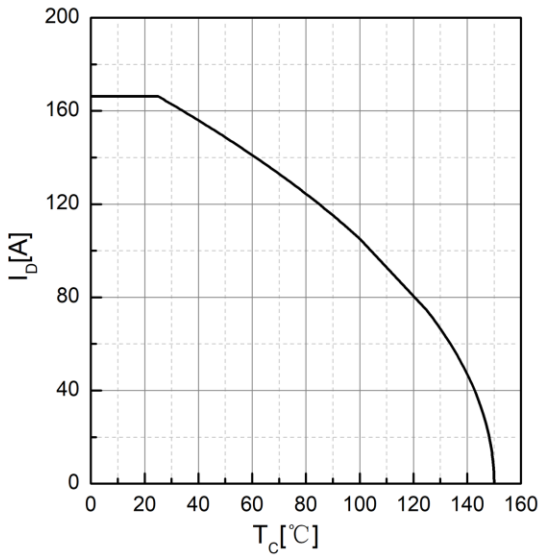


Figure 13. Drain current

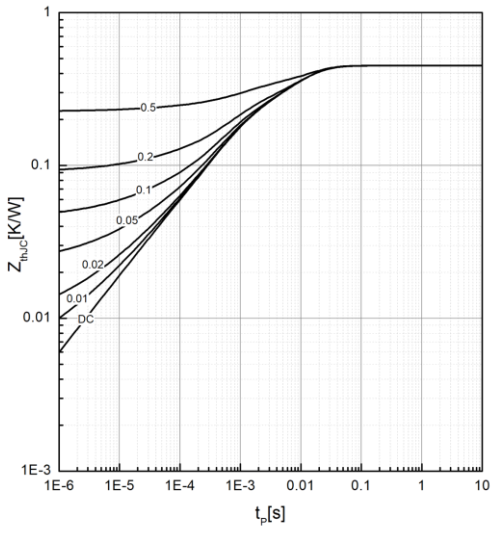


Figure 14. Effective Transient Thermal Impedance

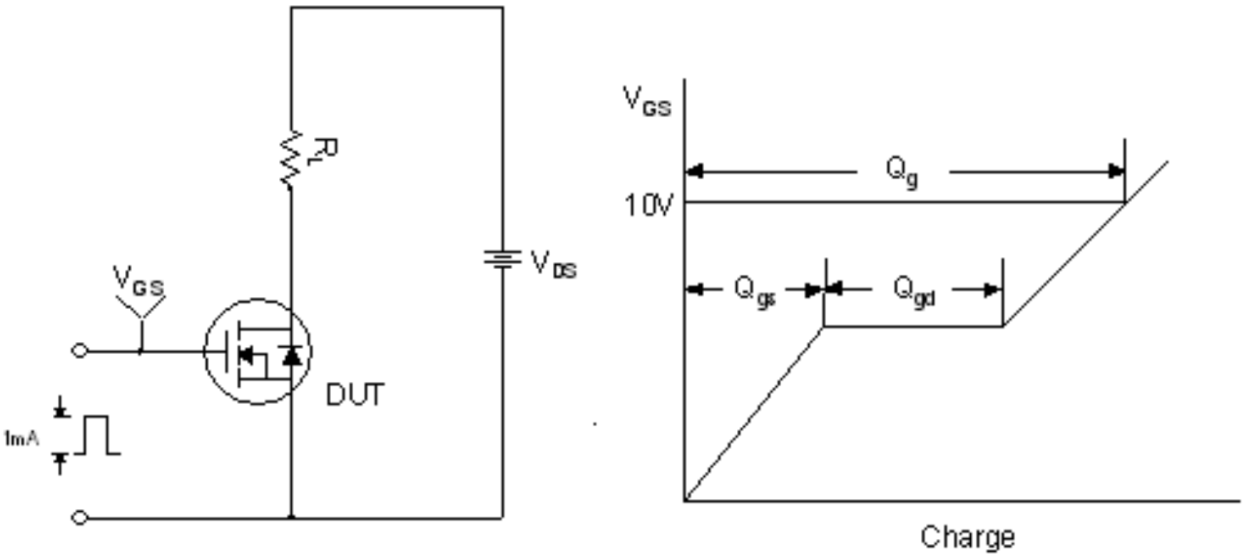


Figure 15. Gate Charge Test Circuit & Waveform

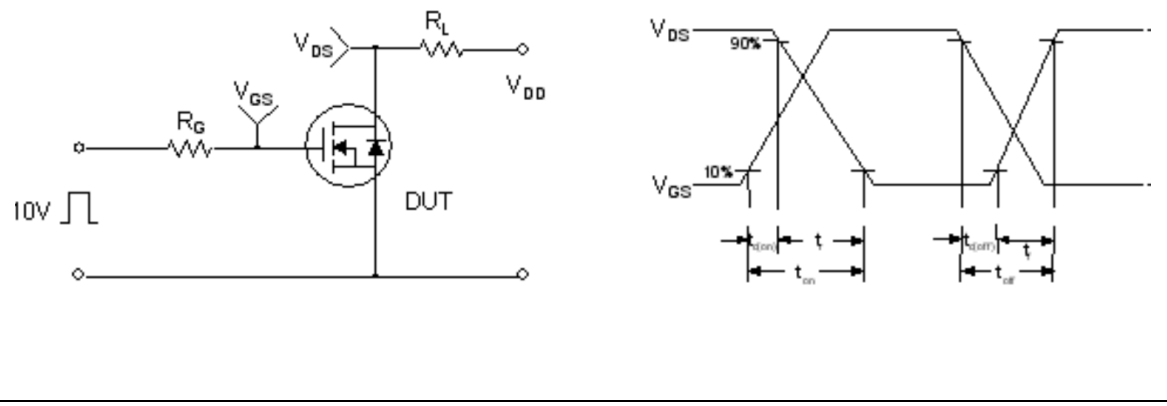


Figure 16. Resistive Switching Test Circuit & Waveforms

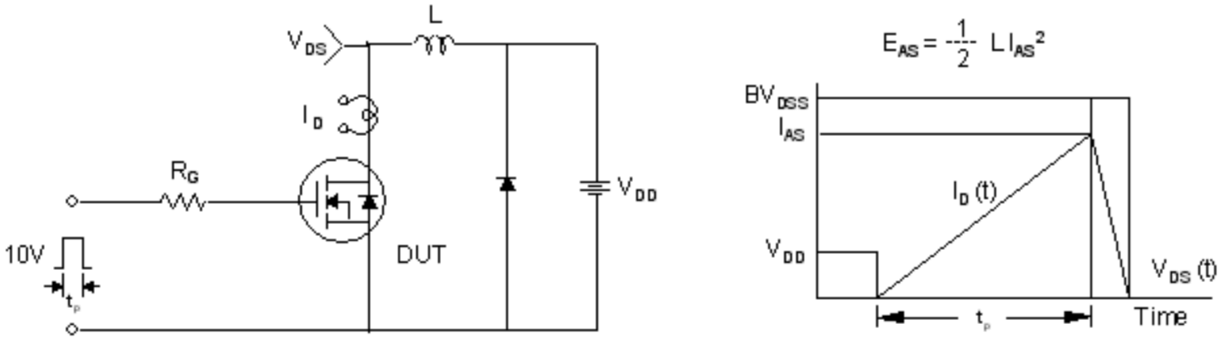


Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms

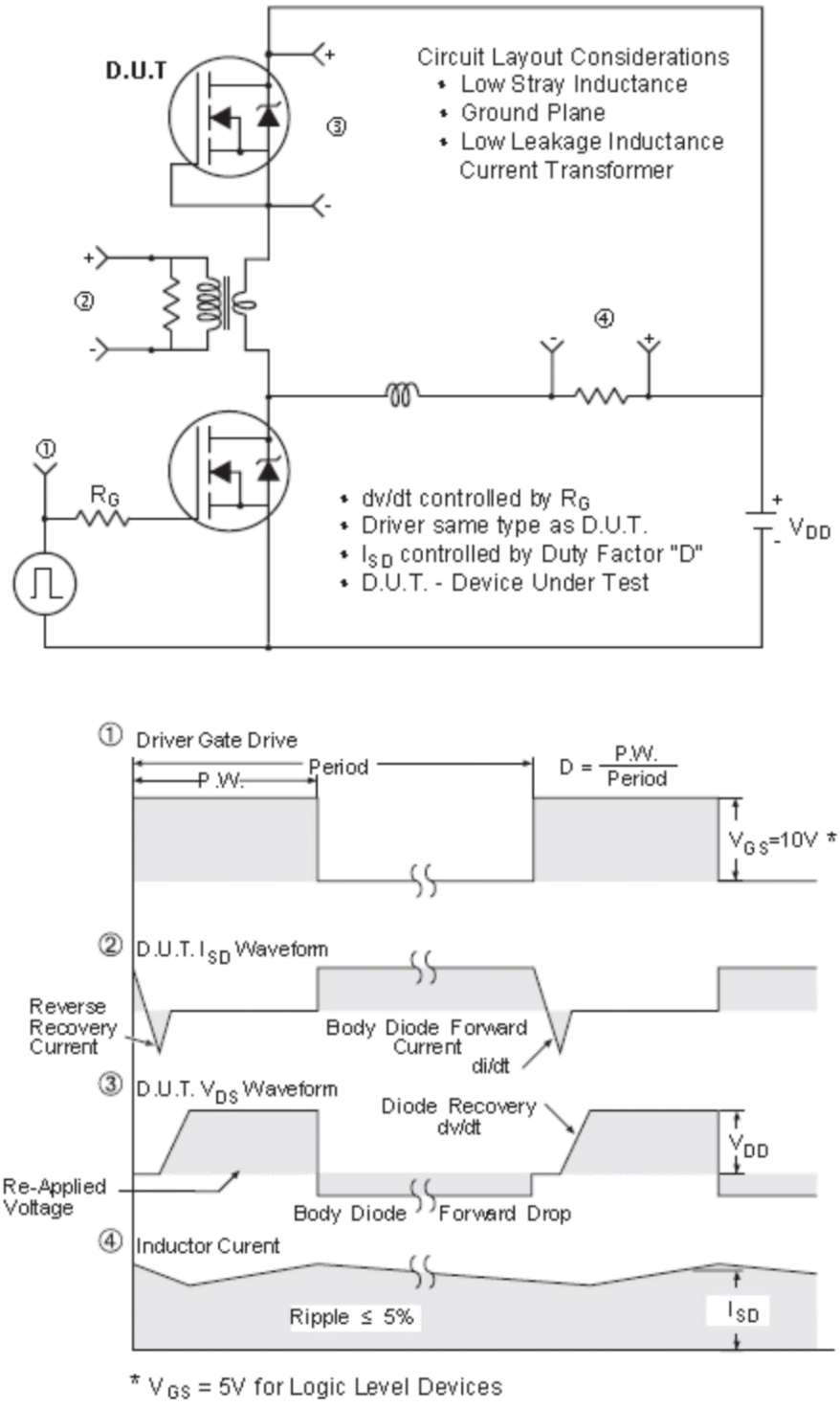
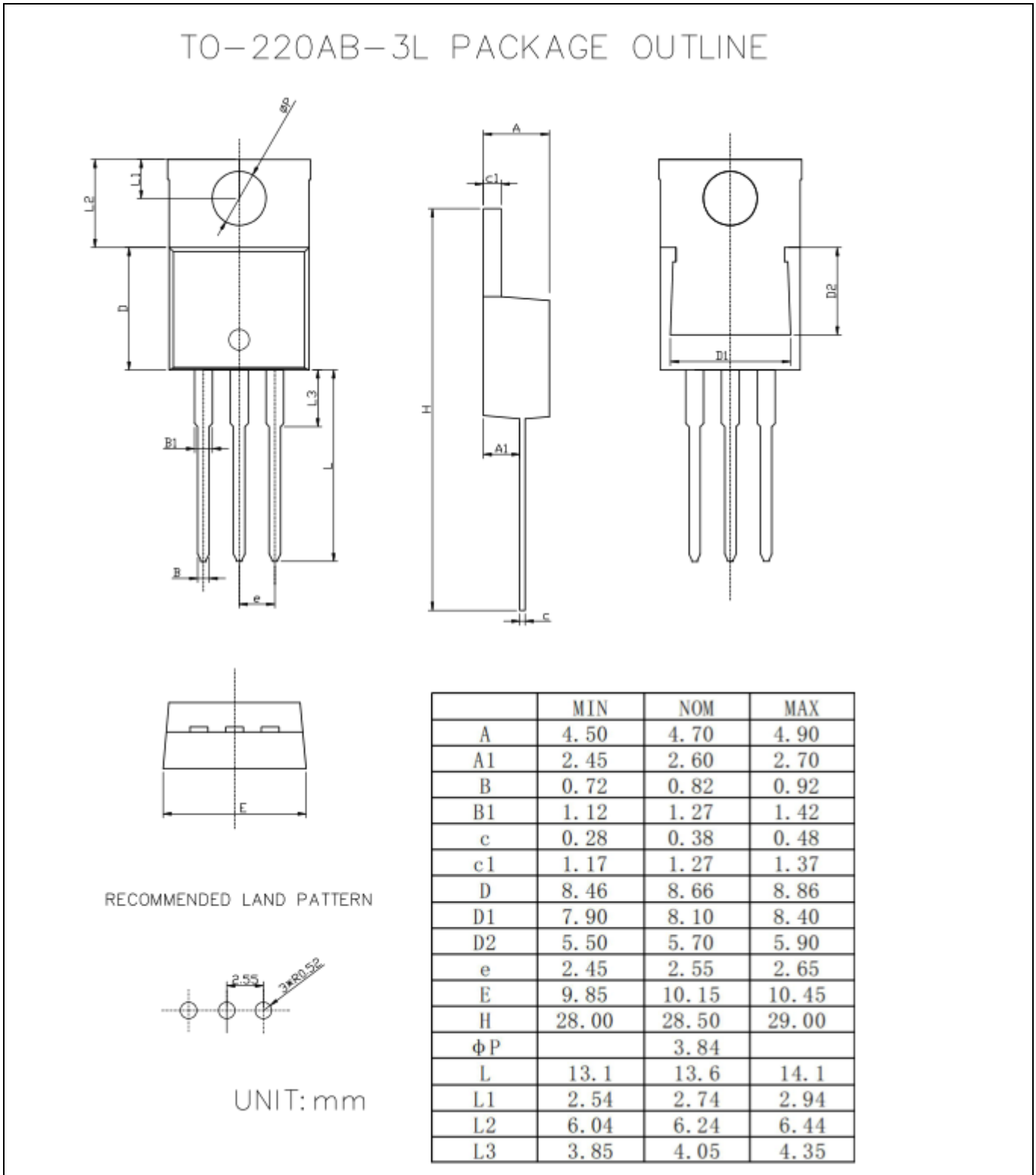


Figure 18. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

Package outline



	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.45	2.60	2.70
B	0.72	0.82	0.92
B1	1.12	1.27	1.42
c	0.28	0.38	0.48
c1	1.17	1.27	1.37
D	8.46	8.66	8.86
D1	7.90	8.10	8.40
D2	5.50	5.70	5.90
e	2.45	2.55	2.65
E	9.85	10.15	10.45
H	28.00	28.50	29.00
ΦP		3.84	
L	13.1	13.6	14.1
L1	2.54	2.74	2.94
L2	6.04	6.24	6.44
L3	3.85	4.05	4.35

Figure 19. TO220-3L Package outline

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