Description

100V N-CHANNEL ENHANCEMENT MODE POWER MOSFET

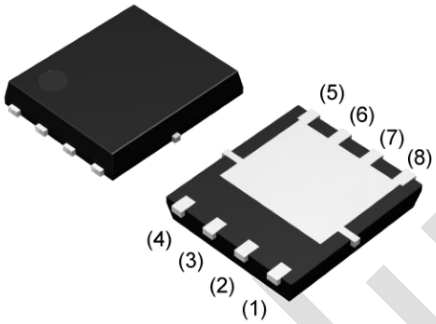
Features

- Device Rating V_{DS} = 100V, I_D = 161A
- $R_{DS(ON)}$ =2.7mΩ (typ.) @ V_{GS} = 10V, I_D = 50A
- Advanced Split Gate Device Design
- RoHS Compliant & Halogen-Free

Application

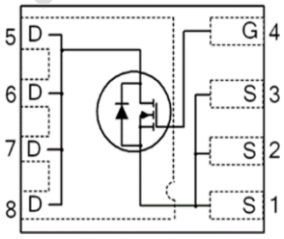
- Brushless DC Motor Control
- DC-DC Converters
- Telecom and Server Power Supply
- High Performance Synchronous Rectification
- Load Switch and eFuse

Package



DFN 5*6-8L

JFG161N100L



Absolute Maximum Ratings T_C=25℃ unless otherwise specified

Symbol	Parameter		Max.	Units
V_{DS}	Drain-Source Voltage		40	V
V_{GS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current, VGS @ 10V note1	T_C = 25℃	161	A
		T_C = 100℃	102	A
I_{DM}	Pulsed Drain Current note2		TBD	A
P_D	Power Dissipation note4	T_C = 25℃	156	W
	Power Dissipation	T_A = 25℃	2.5	W
E_{AS}	Single Pulsed Avalanche Energy note3		TBD	mJ
$R_{\theta JC}$	Thermal Resistance, Junction to Case note1		0.8	℃/W
$R_{\theta JA}$	Junction to Ambient (mounted on 1 inch square PCB)		50	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

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Electrical Characteristics T_C=25℃ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	100	-	-	V
I_{DSS}	Drain-Source Leakage Current	V_{DS} =100V, V_{GS}= 0V, T_C = 25℃	-	-	1	μA
		V_{DS} =100V, V_{GS} = 0V, T_C = 55℃	-	-	10	μA
I_{GSS}	Gate-Source Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-100	-	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1.1	-	2.3	V
$R_{DS(on)}$	Static Drain-Source On-Resistance note2	V_{GS} = 10V, I_D =50A	-	2.7	3.3	mΩ
		V_{GS} = 4.5V, I_D =25A	-	3.7	4.5	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 5V, I_D =50A	-	TBD	-	S
Dynamic Characteristics						
R_g	Gate Resistance		-	TBD	-	Ω
C_{iss}	Input Capacitance	V_{DS} = 50V, V_{GS} = 0V, f = 1MHz	-	3600	-	pF
C_{oss}	Output Capacitance		-	1400	-	pF
C_{rss}	Reverse Transfer Capacitance		-	25	-	pF
Q_g	Total Gate Charge	V_{DS} =50V, I_D = 25A, V_{GS} = 4.5V	-	TBD	-	nC
Q_g	Total Gate Charge	V_{DS} =50V, I_D = 25A, V_{GS} = 10V	-	55	-	nC
Q_{gs}	Gate-Source Charge		-	21	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	18	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50V, I_D = 25A, R_G = 1Ω, V_{GS} = 10V	-	TBD	-	ns
t_r	Turn-On Rise Time		-	TBD	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	TBD	-	ns
t_f	Turn-Off Fall Time		-	TBD	-	ns
Source-Drain Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Diode Forward Current note1,5		-	-	130	A
I_{SM}	Maximum Pulsed Diode Forward Current note2,5		-	-	TBD	A
t_{rr}	Reverse Recovery Time	T_J = 25°C, V_R = 50V, I_F = 25A, V_{GS} = 0V di/dt = 400A/μs	-	TBD	-	ns
Q_{rr}	Reverse Recovery Charge		-	TBD	-	nC
V_{SD} note2	Source to Drain Diode Forward Voltage	T_J = 25°C, I_S = 50A, V_{GS} = 0V	-	0.8	-	V

Note :

1.The data tested by surface mounted on one $inch^2$ FR-4 board with 2OZ copper.

2.The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.

3.The EAS data shows Max. rating. The test condition is L=0.5mH, IAS= TBD A.

4.The power dissipation is limited by 150℃ junction temperature.

5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

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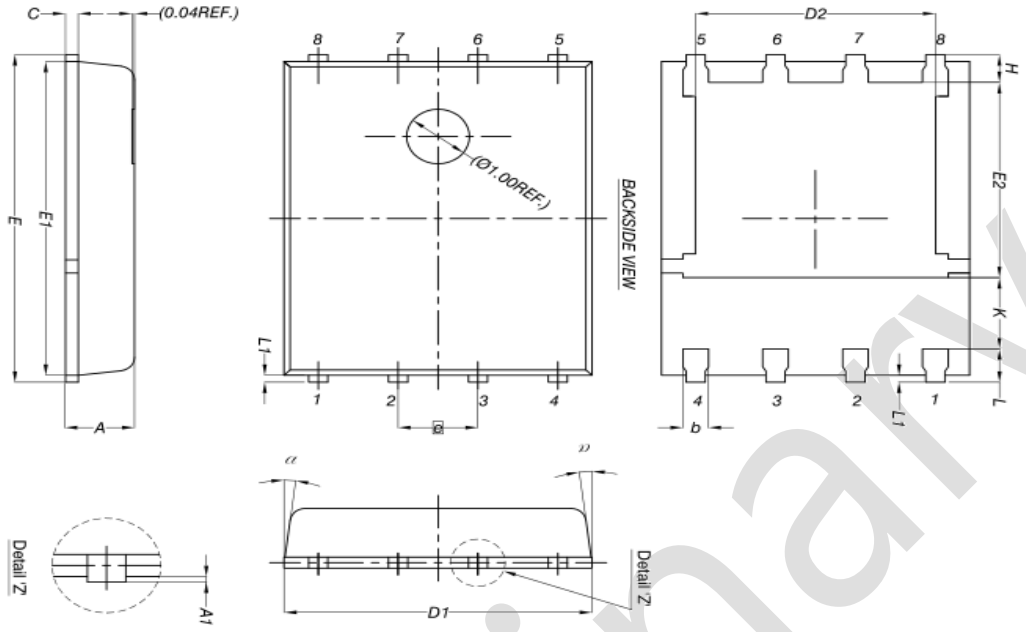
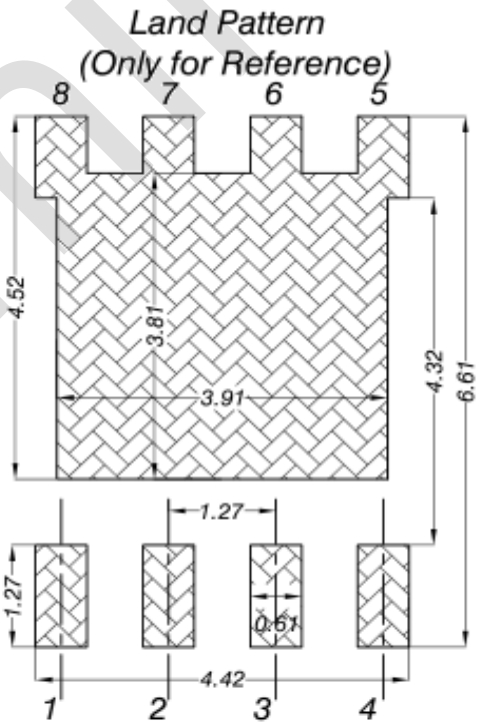
Package outline



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°



Note:
1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar , Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
4. The Package Top May Be Smaller Than The Package Bottom.

Figure 19. DFN 5x6 Package outline

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