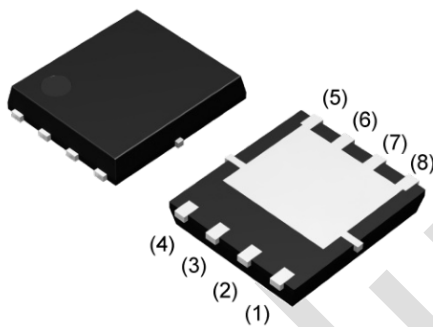


**Description**
**100V N-CHANNEL ENHANCEMENT MODE POWER MOSFET**
**Features**

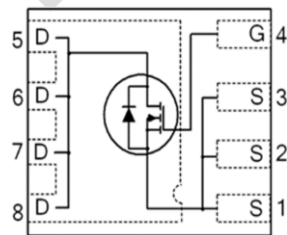
- Device Rating  $V_{DS} = 100V$ ,  $I_D = 160A$
- $R_{DS(ON)} = 2.8m\Omega$  (typ.) @  $V_{GS} = 10V$ ,  $I_D = 50A$
- Advanced Split Gate Device Design
- RoHS Compliant & Halogen-Free

**Application**

- Brushless DC Motor Control
- DC-DC Converters
- Telecom and Server Power Supply
- High Performance Synchronous Rectification
- Load Switch and eFuse

**Package**


**DFN 5\*6-8L**  
**JFG160N100L**


**Absolute Maximum Ratings**  $T_C=25^\circ C$  unless otherwise specified

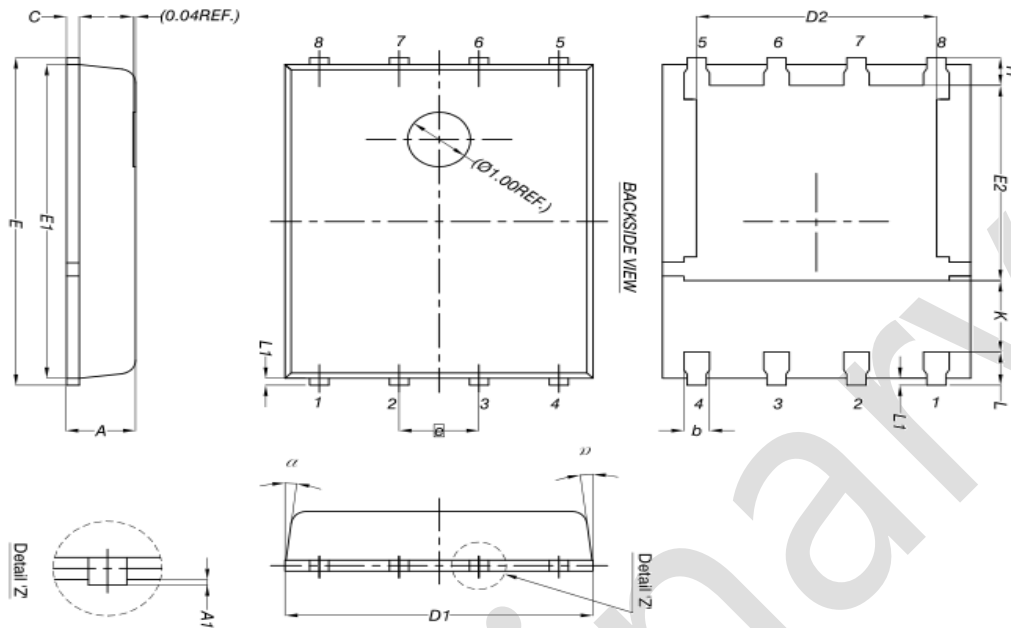
Symbol	Parameter	Max.	Units	
$V_{DS}$	Drain-Source Voltage	40	V	
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V	
$I_D$	Continuous Drain Current, $V_{GS} @ 10V$ <sup>note1</sup>	$T_C = 25^\circ C$	160	A
		$T_C = 100^\circ C$	101	A
$I_{DM}$	Pulsed Drain Current <sup>note2</sup>	TBD	A	
$P_D$	Power Dissipation <sup>note4</sup>	$T_C = 25^\circ C$	156	W
	Power Dissipation	$T_A = 25^\circ C$	2.5	W
$E_{AS}$	Single Pulsed Avalanche Energy <sup>note3</sup>	TBD	mJ	
$R_{\theta JC}$	Thermal Resistance, Junction to Case <sup>note1</sup>	0.8	$^\circ C/W$	
$R_{\theta JA}$	Junction to Ambient (mounted on 1 inch square PCB)	50	$^\circ C/W$	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$	

**Electrical Characteristics**  $T_C=25^\circ\text{C}$  unless otherwise specified

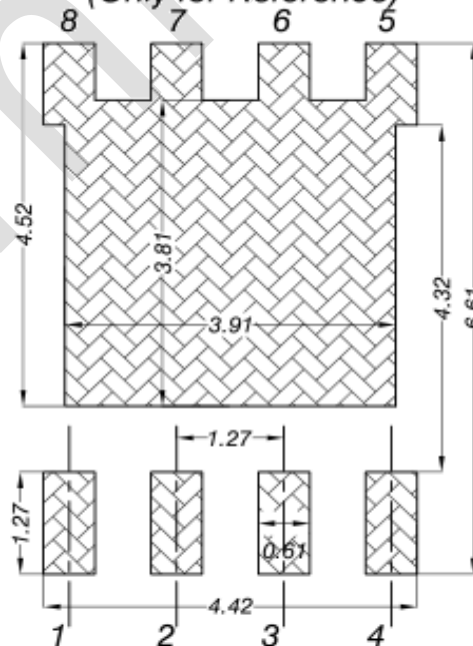
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	100	-	-	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS} = 100V, V_{GS} = 0V, T_C = 25^\circ\text{C}$	-	-	1	$\mu A$
		$V_{DS} = 100V, V_{GS} = 0V, T_C = 55^\circ\text{C}$	-	-	10	$\mu A$
$I_{GSS}$	Gate-Source Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$	-100	-	100	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.3	-	3.3	V
$R_{DS(on)}$	Static Drain-Source On-Resistance <sup>note2</sup>	$V_{GS} = 10V, I_D = 50A$	-	2.8	3.4	m $\Omega$
		$V_{GS} = 8V, I_D = 25A$	-	TBD	TBD	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 5V, I_D = 50A$	-	TBD	-	S
<b>Dynamic Characteristics</b>						
$R_g$	Gate Resistance		-	TBD	-	$\Omega$
$C_{iss}$	Input Capacitance	$V_{DS} = 50V, V_{GS} = 0V,$ $f = 1\text{MHz}$	-	3560	-	pF
$C_{oss}$	Output Capacitance		-	1400	-	pF
$C_{riss}$	Reverse Transfer Capacitance		-	25	-	pF
$Q_g$	Total Gate Charge		-	55	-	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS} = 50V, I_D = 25A,$ $V_{GS} = 10V$	-	21	-	nC
$Q_{gd}$	Gate-Drain("Miller") Charge		-	18	-	nC
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50V, I_D = 25A,$ $R_G = 1\Omega, V_{GS} = 10V$	-	TBD	-	ns
$t_r$	Turn-On Rise Time		-	TBD	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	TBD	-	ns
$t_f$	Turn-Off Fall Time		-	TBD	-	ns
<b>Source-Drain Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Diode Forward Current <sup>note1,5</sup>		-	-	130	A
$I_{SM}$	Maximum Pulsed Diode Forward Current <sup>note2,5</sup>		-	-	TBD	A
$t_{rr}$	Reverse Recovery Time	$T_J = 25^\circ\text{C}, V_R = 50V, I_F = 25A,$ $V_{GS} = 0V, di/dt = 400A/\mu s$	-	TBD	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	TBD	-	nC
$V_{SD}$ <sup>note2</sup>	Source to Drain Diode Forward Voltage	$T_J = 25^\circ\text{C}, I_S = 50A, V_{GS} = 0V$	-	0.8	-	V

Note :

- 1.The data tested by surface mounted on one inch<sup>2</sup> FR-4 board with 20Z copper.
- 2.The data tested by pulsed, pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .
- 3.The EAS data shows Max. rating. The test condition is  $L=0.5\text{mH}$ ,  $I_{AS} = \text{TBD A}$ .
- 4.The power dissipation is limited by  $150^\circ\text{C}$  junction temperature.
- 5.The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.

**Package outline**


DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
$\square$ e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
$\alpha$	0°	-	12°

**Land Pattern  
(Only for Reference)**

**Note:**

1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs.  
Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar , Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
4. The Package Top May Be Smaller Than The Package Bottom.

**Figure 19. DFN 5x6 Package outline**

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