Description

40V N-CHANNEL ENHANCEMENT MODE POWER MOSFET

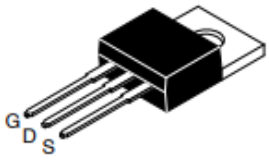
Features

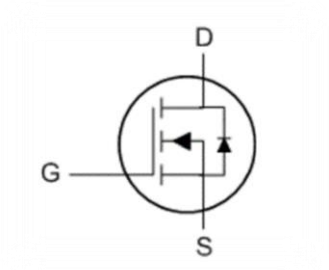
- Device Rating V_{DS} = 40V, I_D = 150A
- $R_{DS(ON)}$ =2.7mΩ (typ.) @ V_{GS} = 10V, I_D = 20A
- Proprietary High Density Trench Technology
- RoHS Compliant & Halogen-Free

Application

- Battery management
- System and Power managerment

Package





TO-220-3L

JFG150N40B

Absolute Maximum Ratings T_C=25℃ unless otherwise specified

Symbol	Parameter		Max.	Units
V_{DS}	Drain-Source Voltage		40	V
V_{GS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current, VGS @ 10V note1	T_C = 25℃	150	A
		T_C = 100℃	95	A
I_{DM}	Pulsed Drain Current note2		600	A
P_D	Power Dissipation note4	T_C = 25℃	104	W
	Power Dissipation	T_A = 25℃	2.15	W
E_{AS}	Single Pulsed Avalanche Energy note3		150	mJ
$R_{\theta JC}$	Thermal Resistance, Junction to Case note1		1.2	℃/W
$R_{\theta JA}$	Junction to Ambient (mounted on 1 inch square PCB)		58	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

Electrical Characteristics T_C=25℃ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	40	-	-	V
I_{DSS}	Drain-Source Leakage Current	V_{DS} = 40V,V_{GS} = 0V, T_C = 25℃	-	-	1	μA
		V_{DS} = 40V,V_{GS} = 0V, T_C = 55℃	-	-	10	μA
I_{GSS}	Gate-Source Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-100	-	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1.0	-	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance note2	V_{GS} = 10V, I_D =20A	-	2.7	3.0	mΩ
$R_{DS(on)}$	Static Drain-Source On-Resistance note2	V_{GS} = 4.5V, I_D =20A	-	4.1	4.9	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10V, I_D =20A	-	114	-	S
Dynamic Characteristics						
R_g	Gate Resistance		-	1.13	-	Ω
C_{iss}	Input Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz	-	3000	-	pF
C_{oss}	Output Capacitance		-	526	-	pF
C_{rss}	Reverse Transfer Capacitance		-	501	-	pF
Q_g	Total Gate Charge	V_{DS} =20V, I_D = 20A, V_{GS} = 10V	-	72.8	-	nC
Q_{gs}	Gate-Source Charge		-	7.61	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	24.6	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 20V, I_D = 20A, R_G = 1Ω, V_{GS} = 10V	-	20	-	ns
t_r	Turn-On Rise Time		-	64	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	70	-	ns
t_f	Turn-Off Fall Time		-	56	-	ns
Source-Drain Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Diode Forward Current note1,5		-	-	86	A
I_{SM}	Maximum Pulsed Diode Forward Current note2,5		-	-	600	A
t_{rr}	Reverse Recovery Time	T_J = 25°C, I_S = 20A, V_{GS} = 0V di/dt = 100A/μs	-	40	-	ns
Q_{rr}	Reverse Recovery Charge		-	20	-	nC
V_{SD} note2	Source to Drain Diode Forward Voltage	T_J = 25°C, I_S = 20A, V_{GS} = 0V	-	0.8	-	V

Note :

1.The data tested by surface mounted on one $inch^2$ FR-4 board with 2OZ copper.

2.The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.

3.The EAS data shows Max. rating. The test condition is L=0.1mH, I_{AS}= 54.9 A.

4.The power dissipation is limited by 150℃ junction temperature.

5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Performance Characteristics

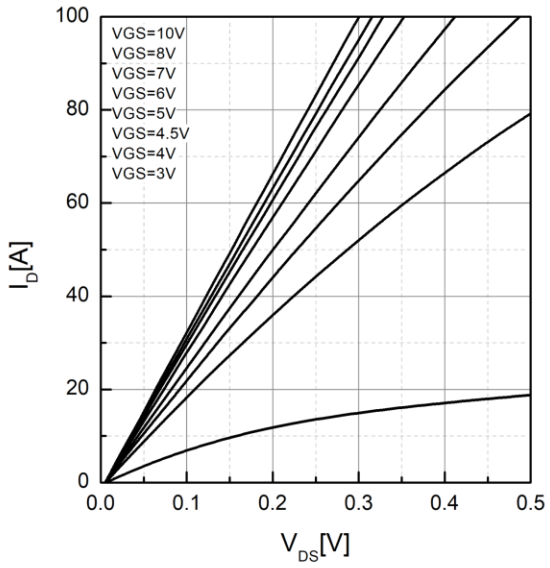


Figure 1. Output Characteristics, TJ=25℃

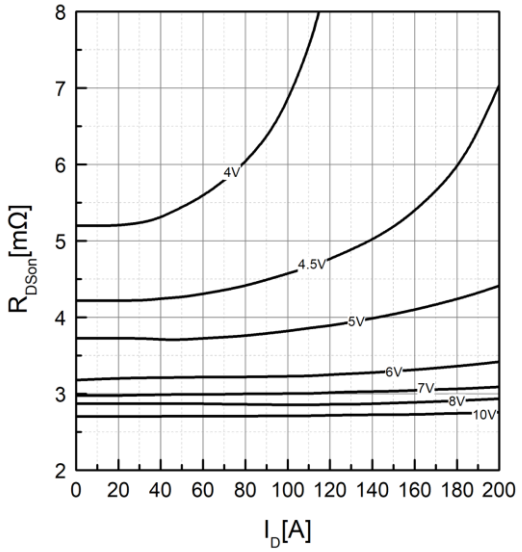


Figure 2. Drain-source on resistance , TJ=25℃

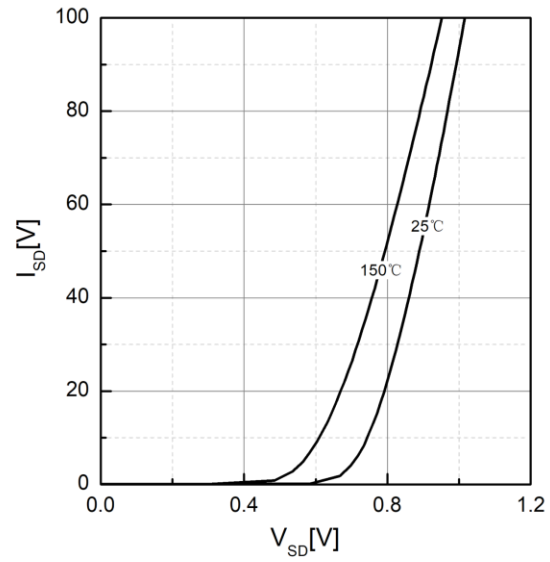


Figure 3. Forward characteristics of body diode

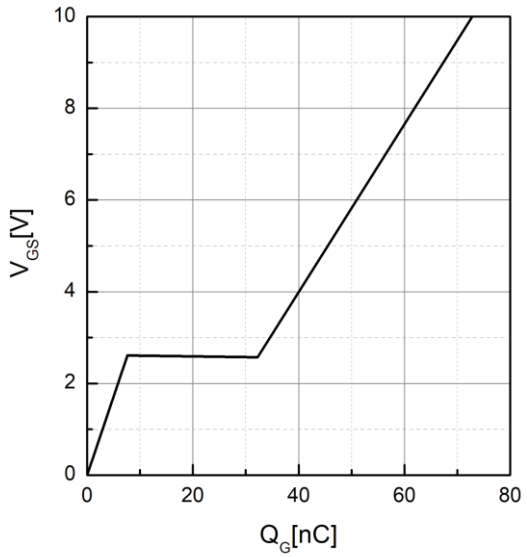


Figure 4. Gate Charge Characteristics

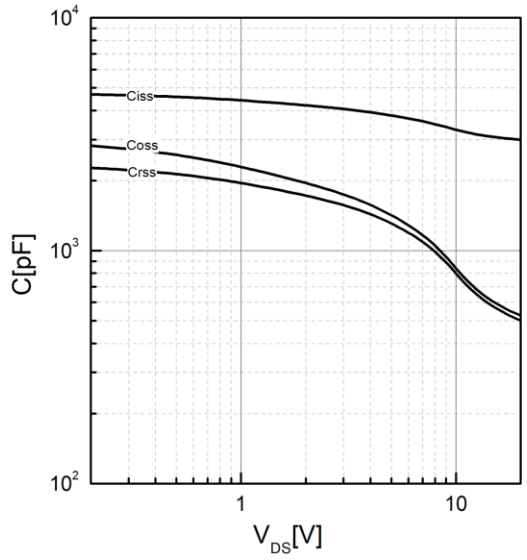


Figure 5. Capacitance Characteristics

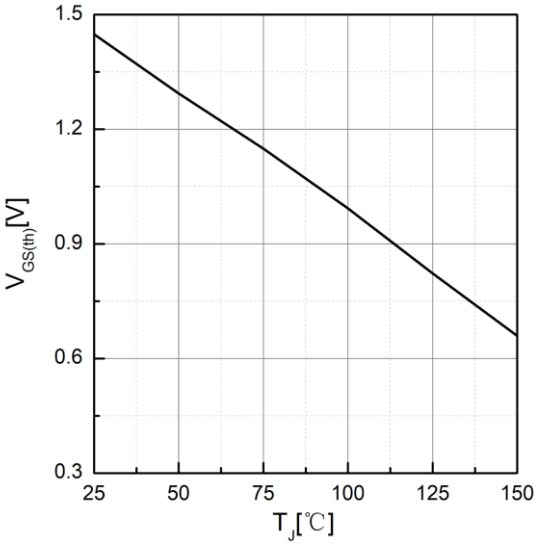


Figure 6. Threshold Voltage Vs. Temperature

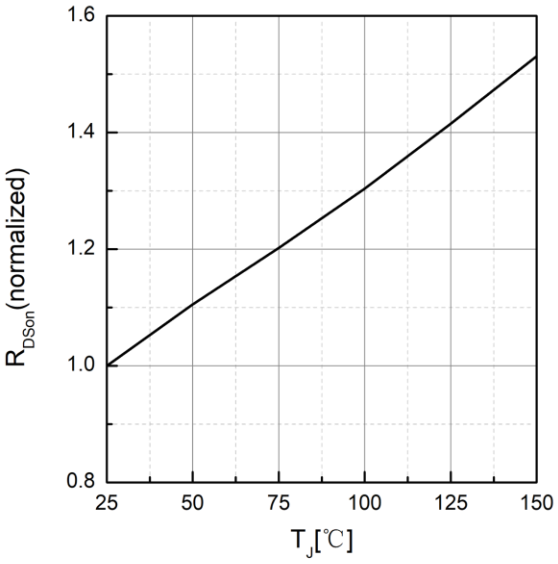


Figure 7. Drain-source on-state resistance

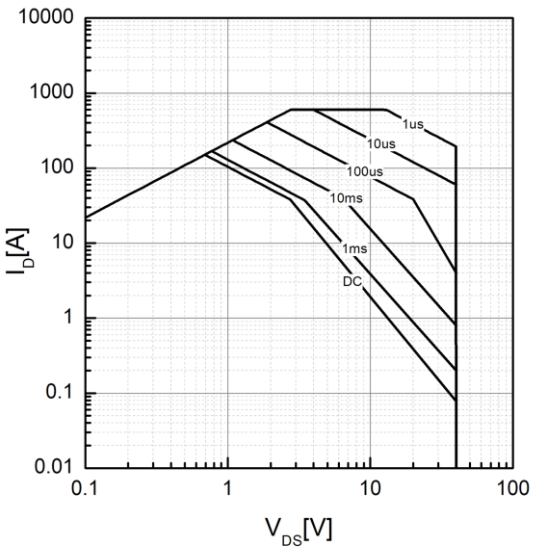


Figure 8. Maximum Safe Operating Area

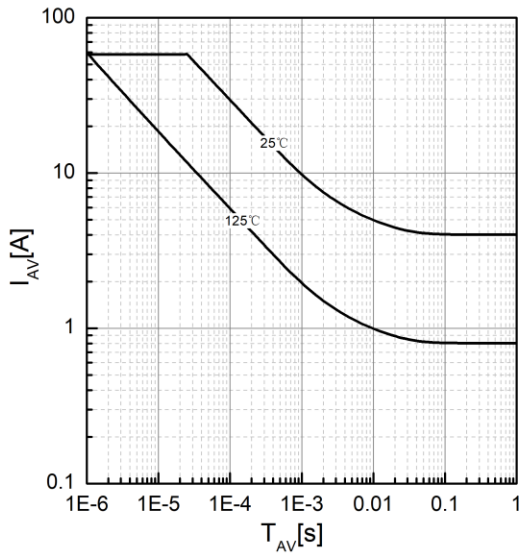


Figure 9. Avalanche characteristics

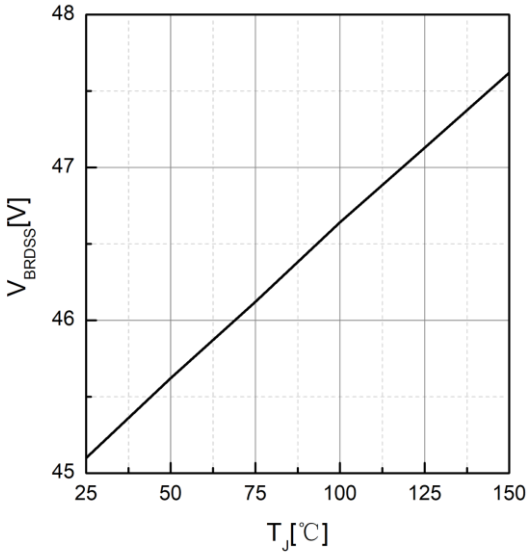


Figure 10. Drain-source breakdown voltage

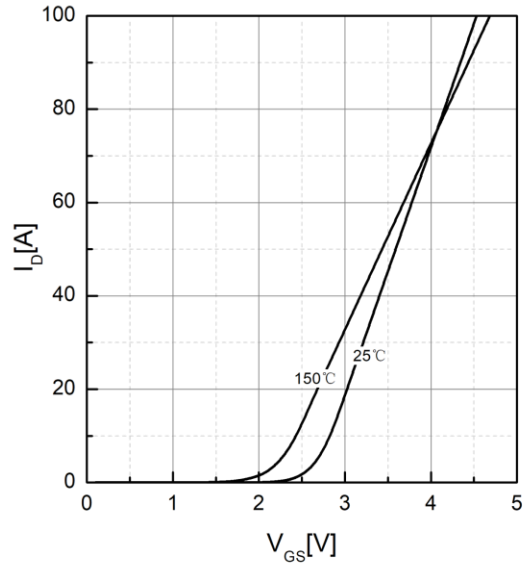


Figure 11. Transfer characteristics

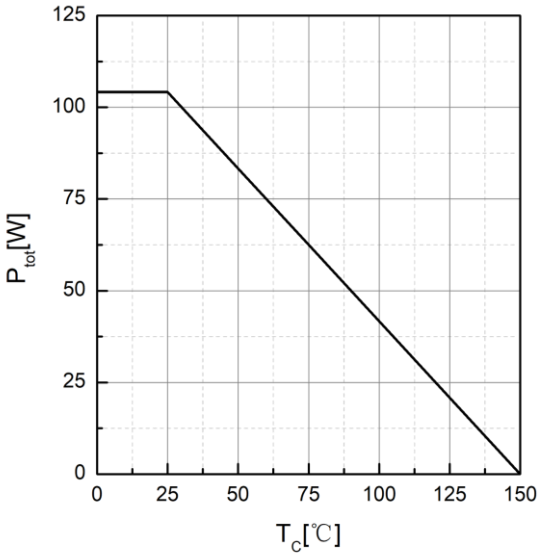


Figure 12. Power dissipation

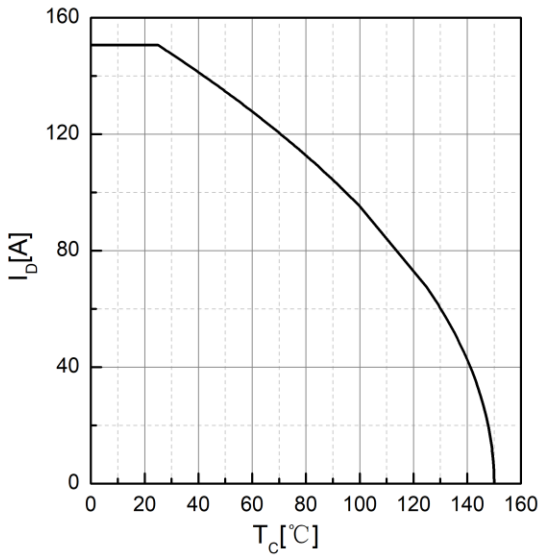


Figure 13. Drain current

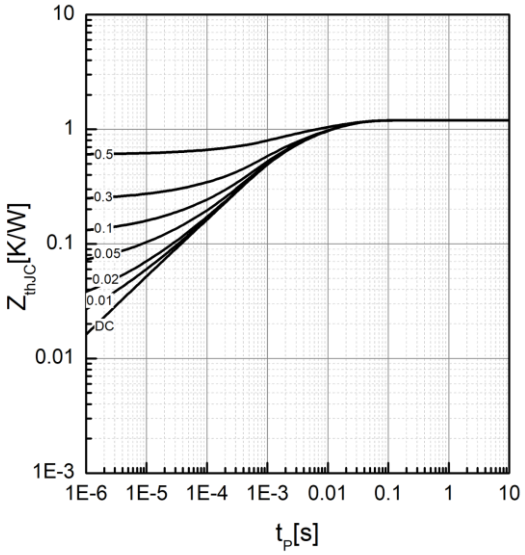


Figure 14. Effective Transient Thermal Impedance

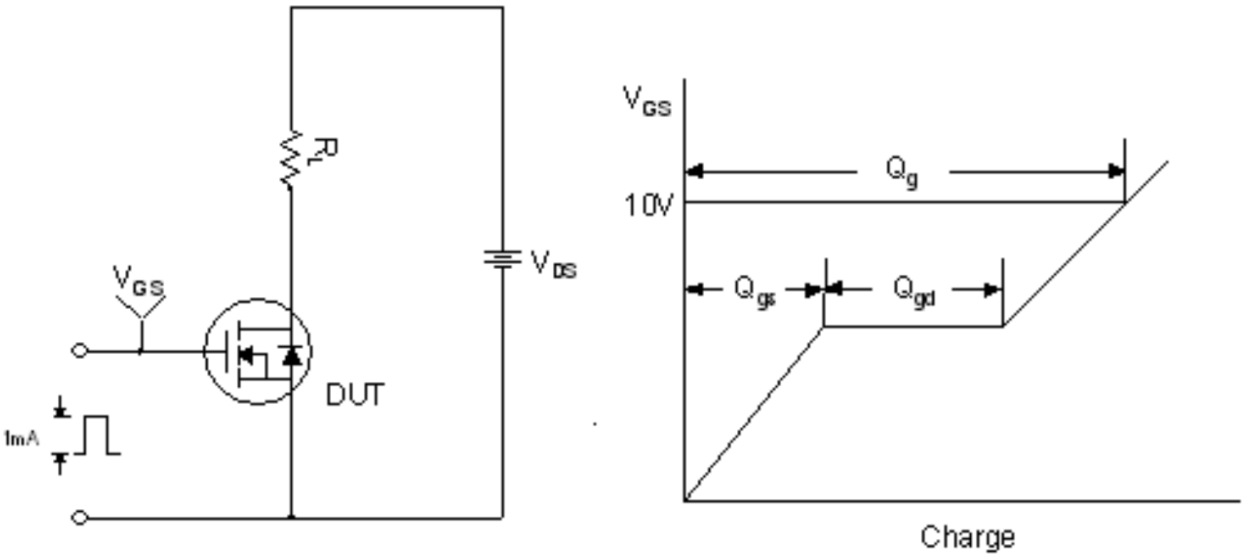


Figure 15. Gate Charge Test Circuit & Waveform

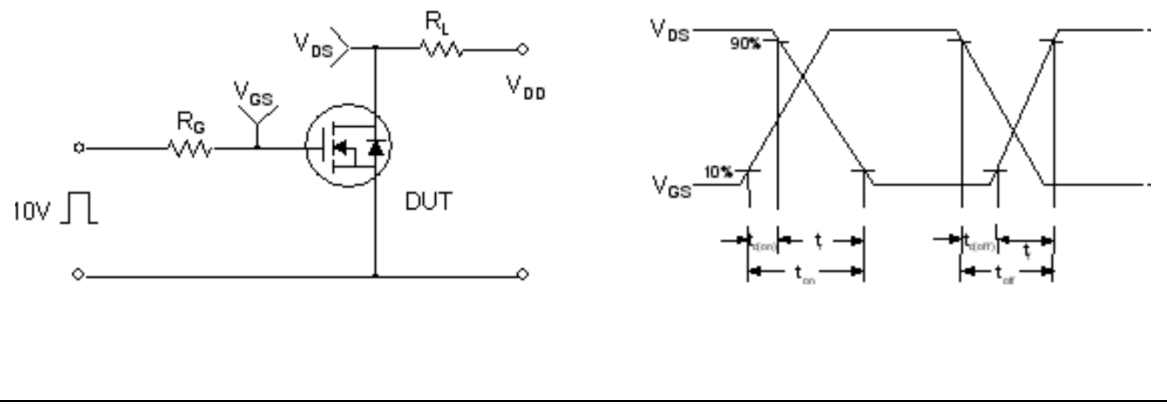


Figure 16. Resistive Switching Test Circuit & Waveforms

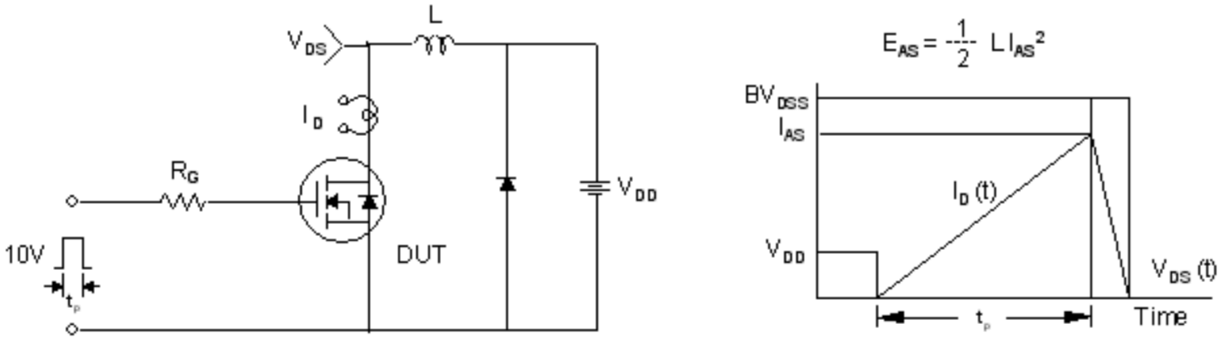


Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms

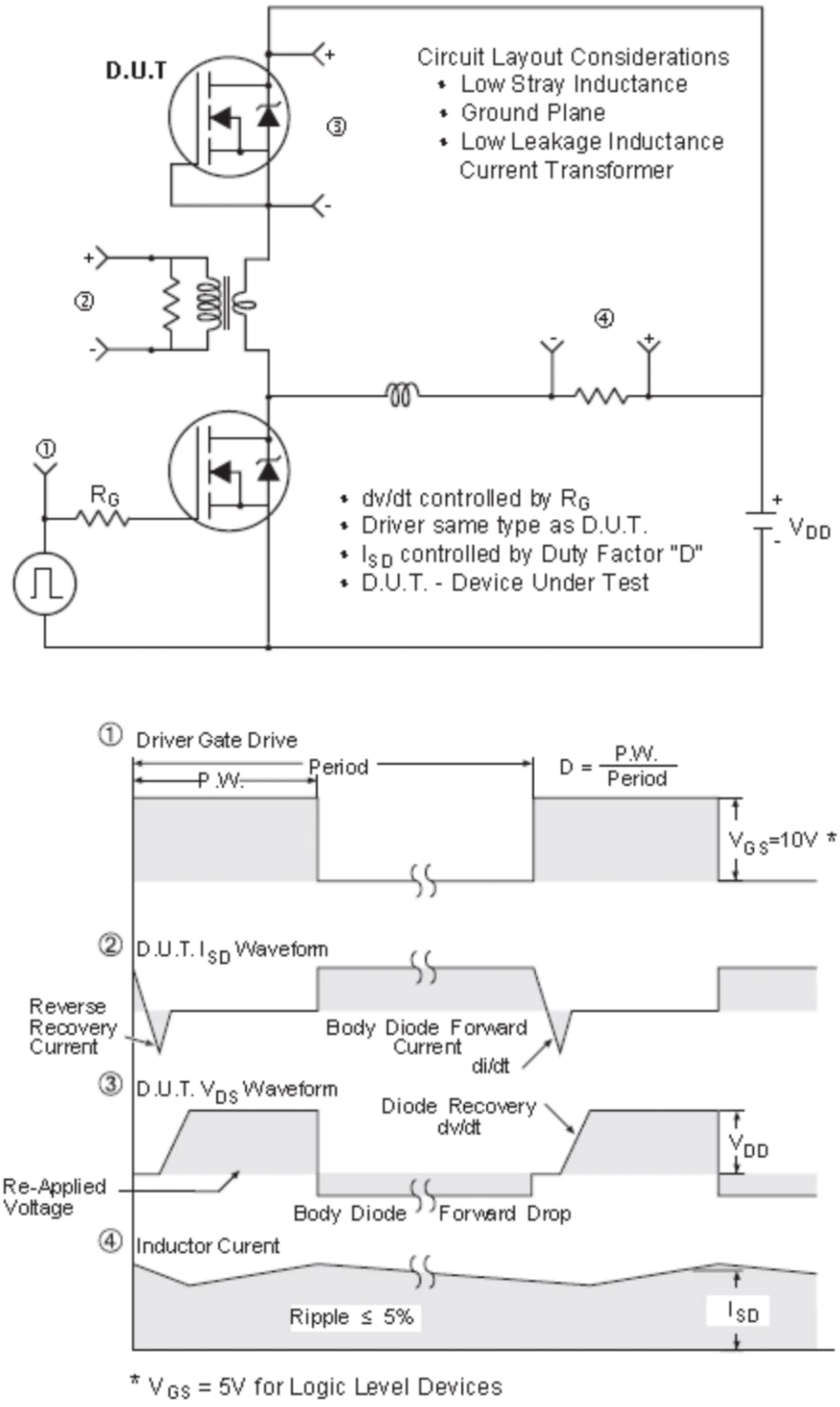
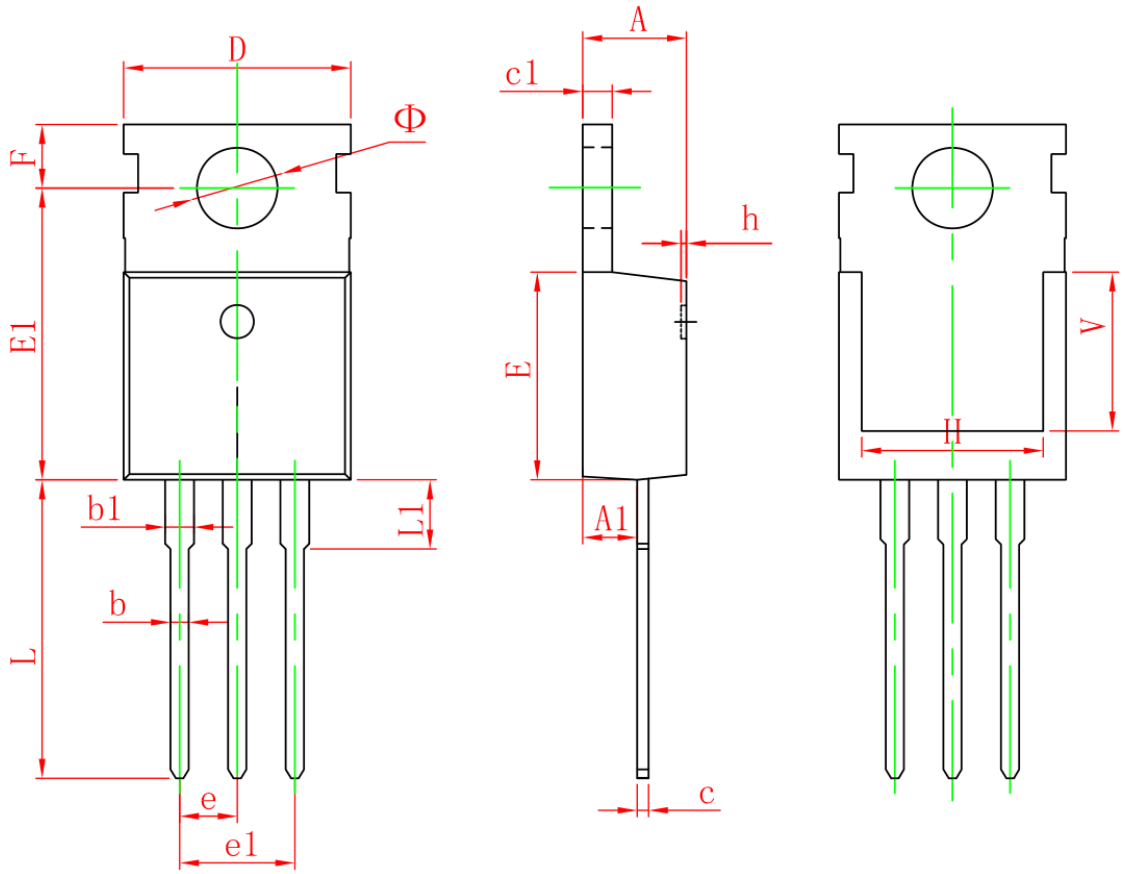


Figure 18. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

Package outline



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.950	9.750	0.352	0.384
E1	12.650	13.050	0.498	0.514
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	6.900 REF.		0.276 REF.	
Φ	3.400	3.800	0.134	0.150

Figure 19. TO220-3L Package outline

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