

Description

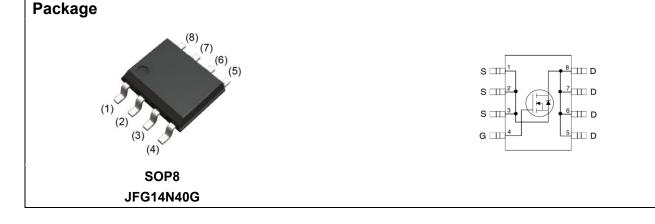
40V N-CHANNEL ENHANCEMENT MODE POWER MOSFET

Features

- Device Rating V_{DS} = 40V, I_D = 14A
- R_{DS(ON)} =5.7mΩ (typ.) @ V_{GS} = 10V, I_D = 8A
- R_{DS(ON)} =8.8mΩ (typ.) @ V_{GS} = 4.5V, I_D = 6A
- Proprietary High Density Trench Technology
- RoHS Compliant & Halogen-Free

Application

• Battery management system and Power managerment



Absolute Maximum Ratings Tc=25°C unless otherwise specified

Symbol	Parameter		Max.	Units
V _{DS}	Drain-Source Voltage		40	V
V _{GS}	Gate-Source Voltage		± 20	V
ID	Continuous Drain Current, VGS @ 10V ^{note1}	T _A = 25°C	14	А
		T _A = 70°C	11	А
IDM	Pulsed Drain Current note2		115	А
P _D	Power Dissipation note4	T _A = 25°C	2.15	W
	Power Dissipation	T _A = 70°C	1.37	W
Eas	Single Pulsed Avalanche Energy note3		39	mJ
Rejl	Thermal Resistance, Junction to Lead note1		20	°C/W
Reja	Junction to Ambient (mounted on 1 inch square PCB)		58	°C/W
TJ, TSTG	Operating and Storage Temperature Range		-55 to +150	°C



Electrical Characteristics Tc=25°C unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Units
Off Charac	teristic		•			
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250µA	40	-	-	V
IDSS	Drain-Source Leakage Current	V _{DS} = 40V, V _{GS} = 0V, T _C = 25°C	-	-	1	μA
		V _{DS} = 40V, V _{GS} = 0V, T _C = 55°C	-	-	10	μA
I _{GSS}	Gate-Source Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-100	-	100	nA
On Charac	teristics					
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250µA	1.0	-	2.5	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10V, I _D =8A	-	5.7	6.9	mΩ
		V _{GS} = 4.5V, I _D =6A	-	8.8	10.6	mΩ
g fs	Forward Transconductance	V _{DS} = 10V, I _D =8A		46	-	S
Dynamic C	Characteristics					
R _g	Gate Resistance		-	1.68	-	Ω
Ciss	Input Capacitance		-	1070	-	pF
Coss	Output Capacitance	$V_{DS} = 20V, V_{GS} = 0V,$	-	190	-	pF
C _{rss}	Reverse Transfer Capacitance	f = 1MHz	-	182	-	pF
Qg	Total Gate Charge		-	26	-	nC
Q _{gs}	Gate-Source Charge	$V_{DS} = 20V, I_D = 8A,$	-	2.87	-	nC
Q _{gd}	Gate-Drain("Miller") Charge	V _{GS} = 10V	-	9.40	-	nC
Switching	Characteristics					
t _{d(on)}	Turn-On Delay Time		-	14	-	ns
tr	Turn-On Rise Time	V_{DD} = 20V, I_D = 8A, R _G = 1Ω, V _{GS} = 10V	-	36	-	ns
t _{d(off)}	Turn-Off Delay Time		-	40	-	ns
t _f	Turn-Off Fall Time		-	28	-	ns
Source-Dr	ain Diode Characteristics and Maxin	num Ratings				
ls	Maximum Continuous Diode Forward Current note1,5		-	-	1.79	А
I _{SM}	Maximum Pulsed Diode Forward Current note2,5		-	-	115	А
t _{rr}	Reverse Recovery Time	T _J = 25°C, I _S = 8A, V _{GS} = 0V	-	32	-	ns
Qrr	Reverse Recovery Charge	T _J = 25°C, I _S = 8A,		30		nC
		di/dt = 100A/µs				
V_{SD} ^{note2}	Source to Drain Diode Forward Voltage	T _J = 25°C, Is = 8A, V _{GS} = 0V	-	0.79	-	V

Note :

1. The data tested by surface mounted on one inch² FR-4 board with 2OZ copper.

2.The data tested by pulsed, pulse width \leq 300us, duty cycle \leq 2%.

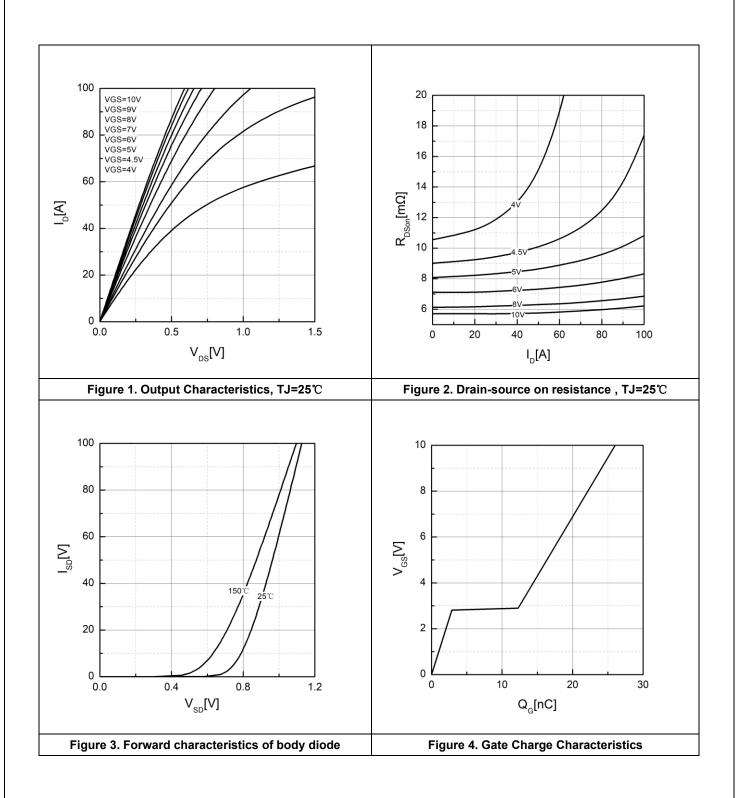
3.The EAS data shows Max. rating. The test condition is L=0.1mH, I_{AS}=27.9 A.

4.The power dissipation is limited by 150°C junction temperature.

5. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

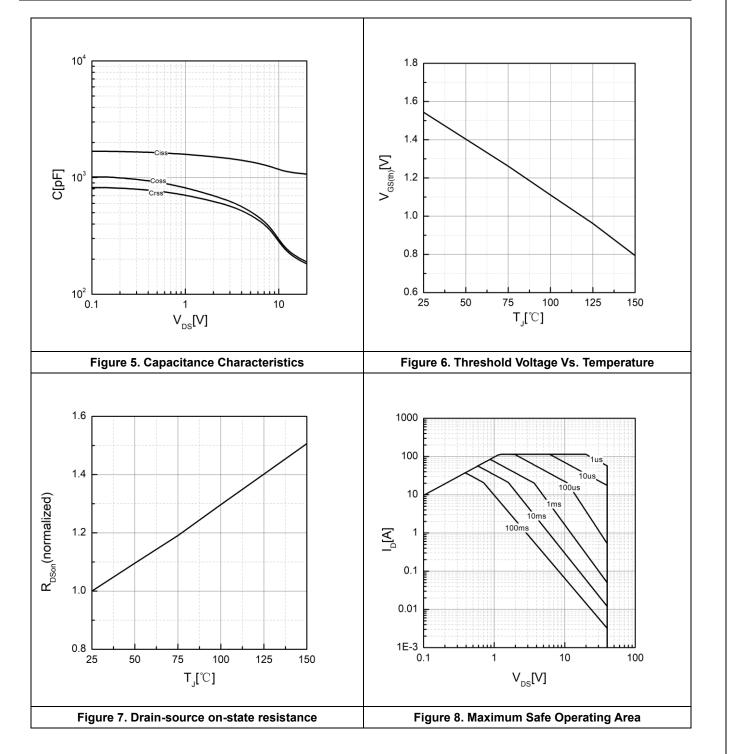


Typical Performance Characteristics



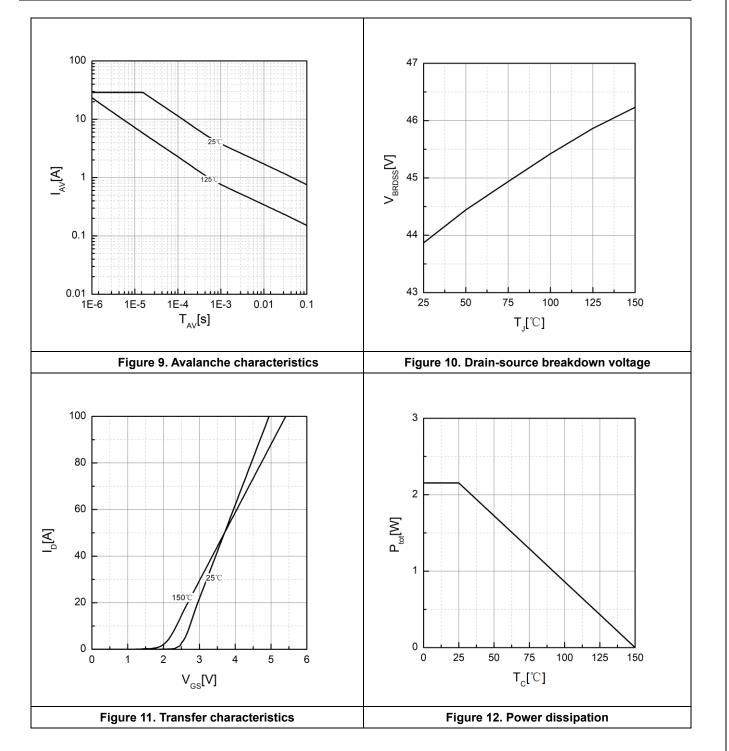


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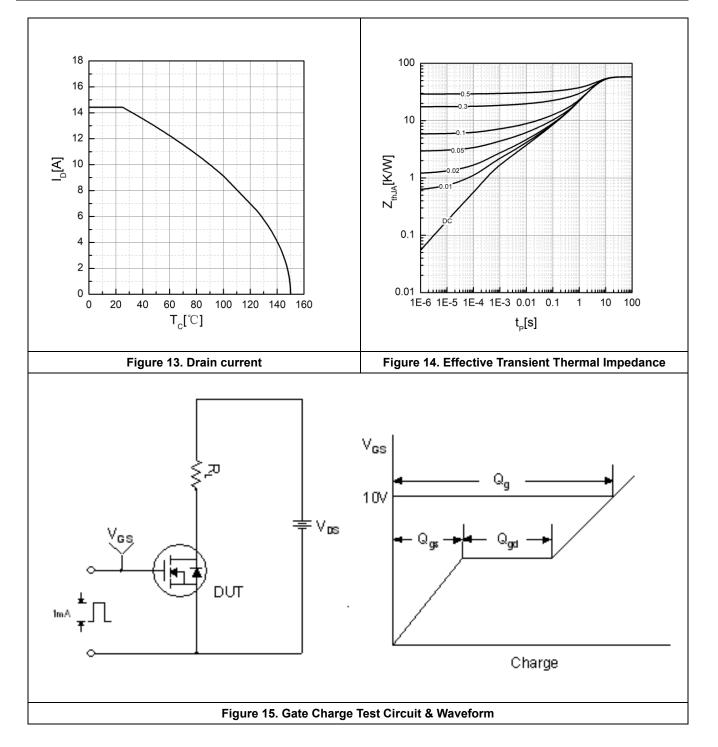


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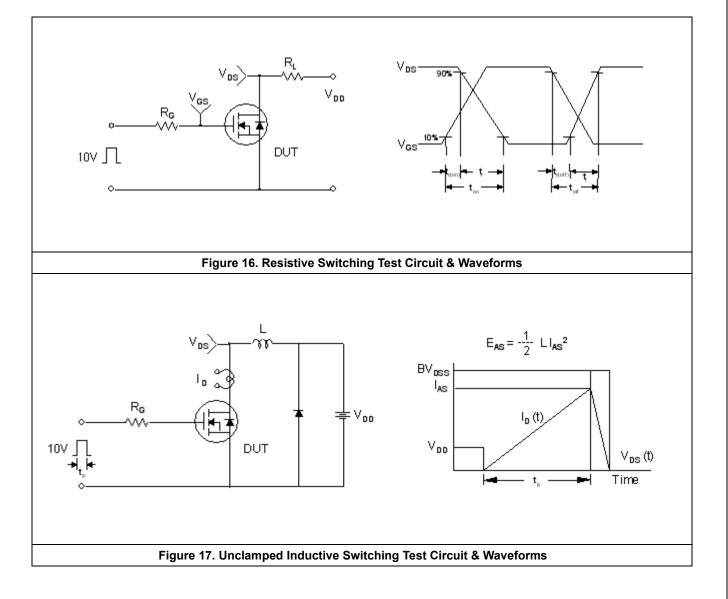






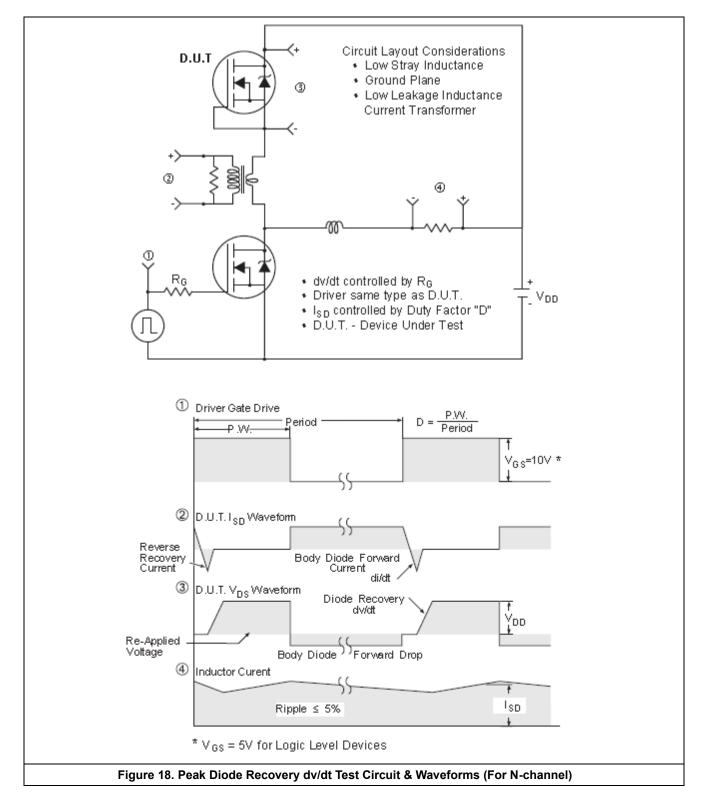






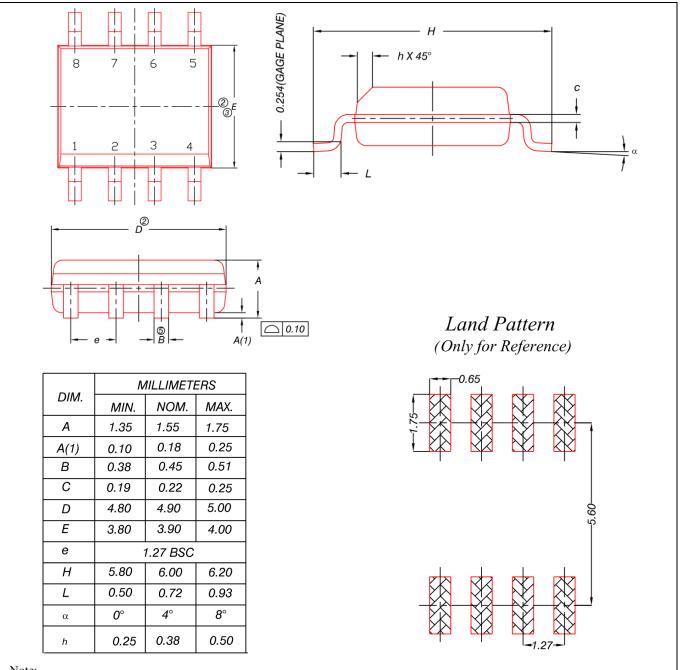


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Package outline



Note:

1. All Dimension Are In mm.

2 Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs.

Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.

- Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
 The Package Top May Be Smaller Than The Package Bottom.
- Dimension "B" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.08 mm Total In Excess Of "B" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.

Figure 19. SOP8 Package outline





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