Description

40V N-CHANNEL ENHANCEMENT MODE POWER MOSFET

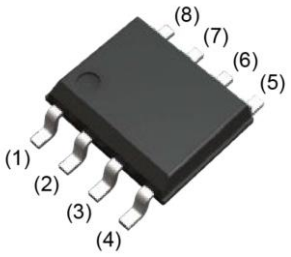
Features

- Device Rating V_{DS} = 40V, I_D = 12A
- $R_{DS(ON)}$ =7.9mΩ (typ.) @ V_{GS} = 10V, I_D = 8A
- $R_{DS(ON)}$ =12.5mΩ (typ.) @ V_{GS} = 4.5V, I_D = 6A
- Proprietary High Density Trench Technology
- RoHS Compliant & Halogen-Free

Application

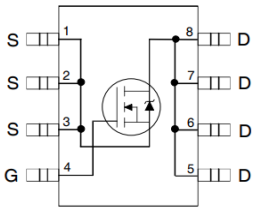
- Battery management system and Power management

Package



SOP8

JFG12N40G



Absolute Maximum Ratings T_C=25℃ unless otherwise specified

Symbol	Parameter		Max.	Units
V_{DS}	Drain-Source Voltage		40	V
V_{GS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current, VGS @ 10V note1	T_A = 25℃	12	A
		T_A = 70℃	9	A
I_{DM}	Pulsed Drain Current note2		96	A
P_D	Power Dissipation note4	T_A = 25℃	2.15	W
	Power Dissipation	T_A = 70℃	0.86	W
E_{AS}	Single Pulsed Avalanche Energy note3		24	mJ
$R_{\theta JL}$	Thermal Resistance, Junction to Lead note1		20	℃/W
$R_{\theta JA}$	Junction to Ambient (mounted on 1 inch square PCB)		58	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

Electrical Characteristics T_C=25℃ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	40	-	-	V
I_{DSS}	Drain-Source Leakage Current	V_{DS} = 40V, V_{GS} = 0V, T_C = 25℃	-	-	1	μA
		V_{DS} = 40V, V_{GS} = 0V, T_C = 55℃	-	-	10	μA
I_{GSS}	Gate-Source Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-100	-	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1.0	-	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance note2	V_{GS} = 10V, I_D =8A	-	7.9	9.5	mΩ
		V_{GS} = 4.5V, I_D =6A	-	12.5	15	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10V, I_D =8A		40	-	S
Dynamic Characteristics						
R_g	Gate Resistance		-	1.7	-	Ω
C_{iss}	Input Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz	-	682	-	pF
C_{oss}	Output Capacitance		-	133	-	pF
C_{rss}	Reverse Transfer Capacitance		-	127	-	pF
Q_g	Total Gate Charge	V_{DS} =20V, I_D = 8A, V_{GS} = 10V	-	16.3	-	nC
Q_{gs}	Gate-Source Charge		-	1.67	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	6.07	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 20V, I_D = 8A, R_G = 1Ω, V_{GS} = 10V	-	9	-	ns
t_r	Turn-On Rise Time		-	27	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	36	-	ns
t_f	Turn-Off Fall Time		-	17	-	ns
Source-Drain Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Diode Forward Current note1,5		-	-	1.79	A
I_{SM}	Maximum Pulsed Diode Forward Current note2,5		-	-	96	A
t_{rr}	Reverse Recovery Time	T_J = 25°C, I_S = 8A, V_{GS} = 0V	-	40	-	ns
Q_{rr}	Reverse Recovery Charge	T_J = 25°C, I_S = 8A, di/dt = 100A/μs		8		nC
V_{SD} note2	Source to Drain Diode Forward Voltage	T_J = 25°C, I_S = 8A, V_{GS} = 0V	-	0.79	-	V

Note :

1.The data tested by surface mounted on one $inch^2$ FR-4 board with 2OZ copper.

2.The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.

3.The EAS data shows Max. rating. The test condition is L=0.1mH, I_{AS}=21.9A.

4.The power dissipation is limited by 150℃ junction temperature.

5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Performance Characteristics

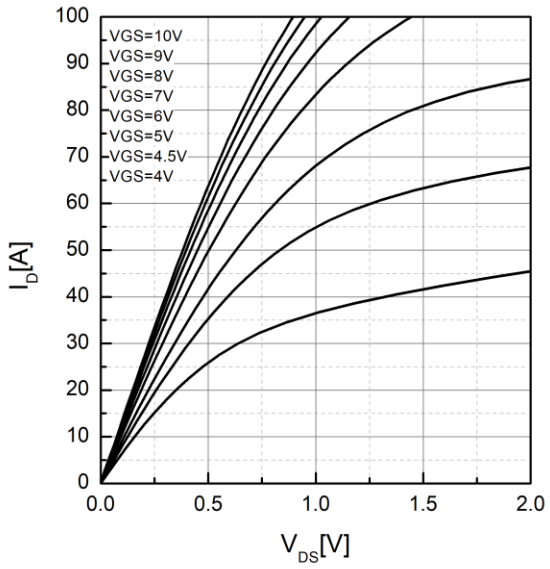


Figure 1. Output Characteristics, TJ=25℃

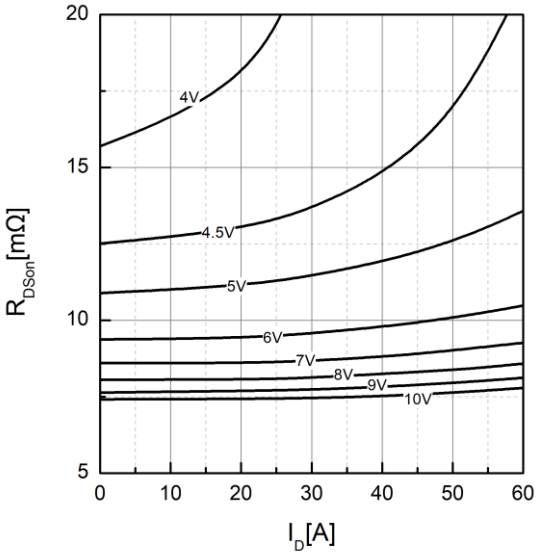


Figure 2. Drain-source on resistance , TJ=25℃

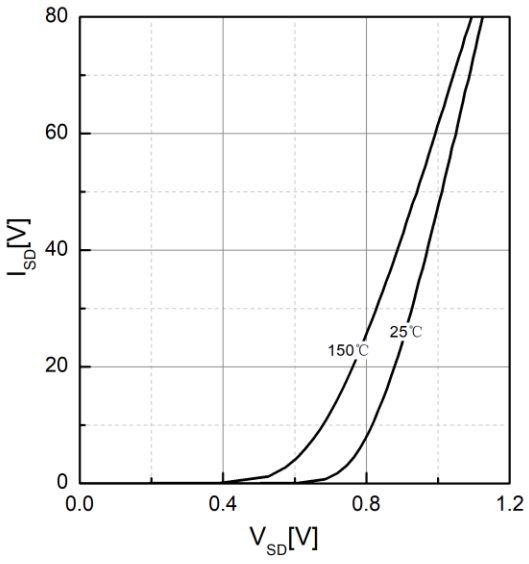


Figure 3. Forward characteristics of body diode

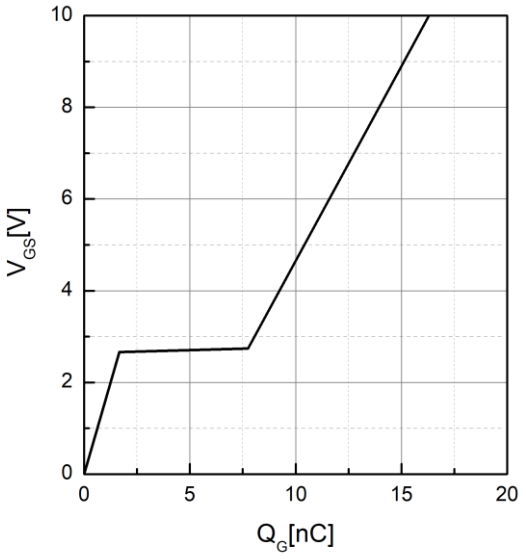


Figure 4. Gate Charge Characteristics

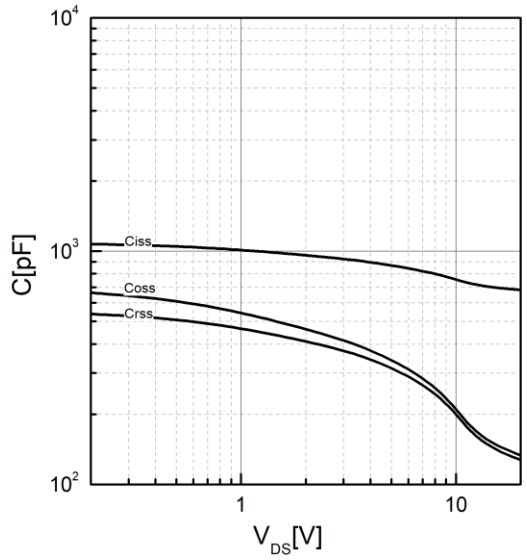


Figure 5. Capacitance Characteristics

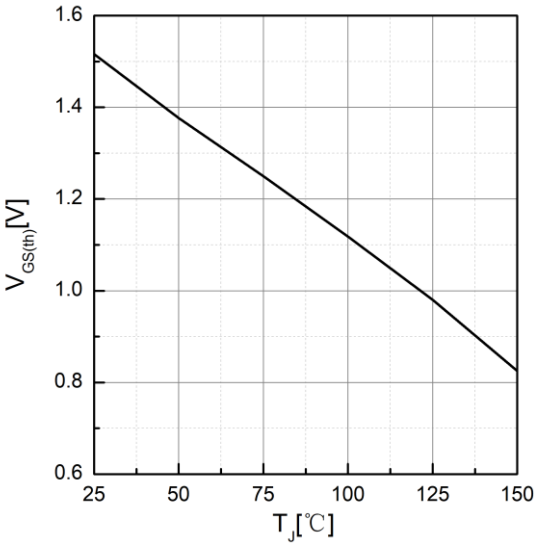


Figure 6. Threshold Voltage Vs. Temperature

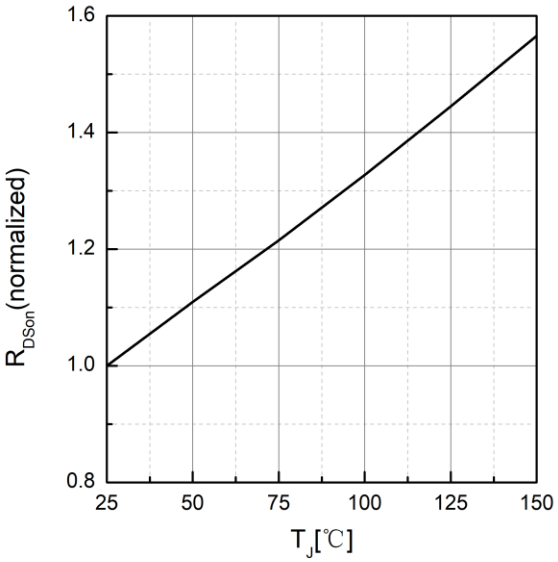


Figure 7. Drain-source on-state resistance

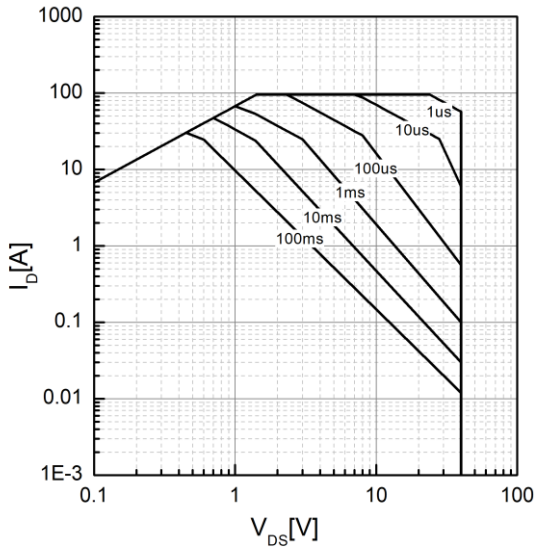


Figure 8. Maximum Safe Operating Area

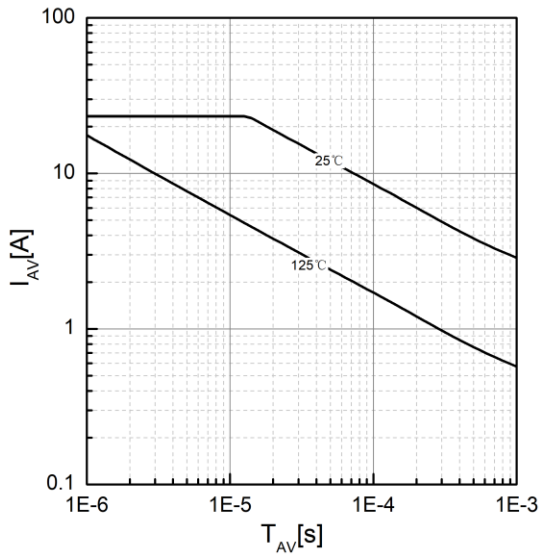


Figure 9. Avalanche characteristics

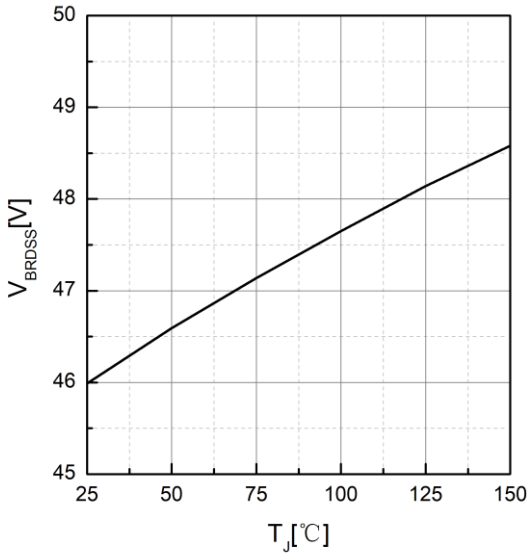


Figure 10. Drain-source breakdown voltage

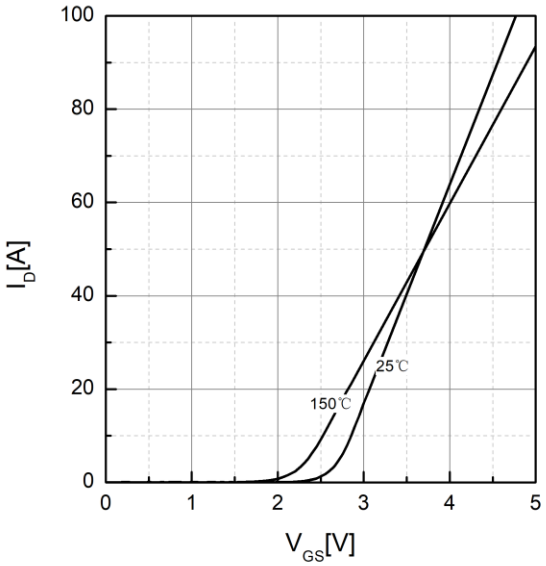


Figure 11. Transfer characteristics

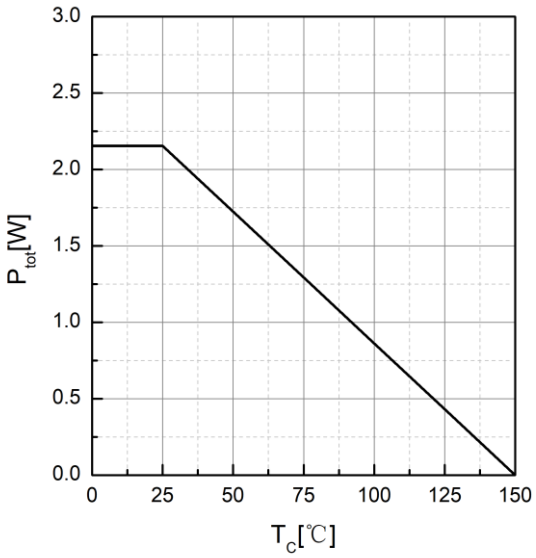


Figure 12. Power dissipation

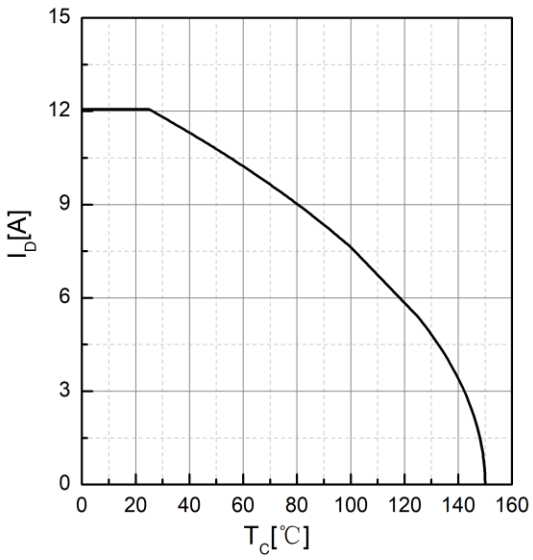


Figure 13. Drain current

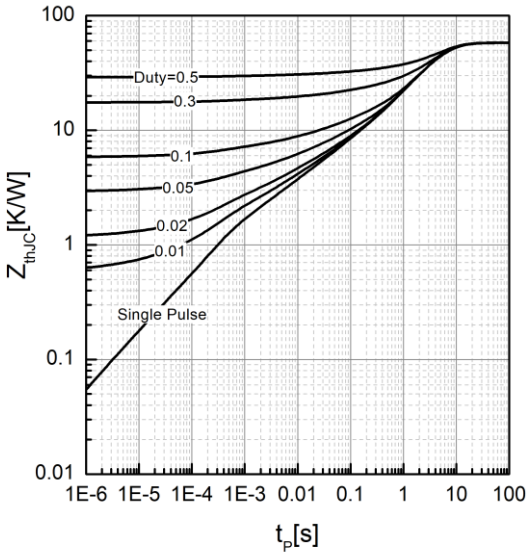


Figure 14. Effective Transient Thermal Impedance

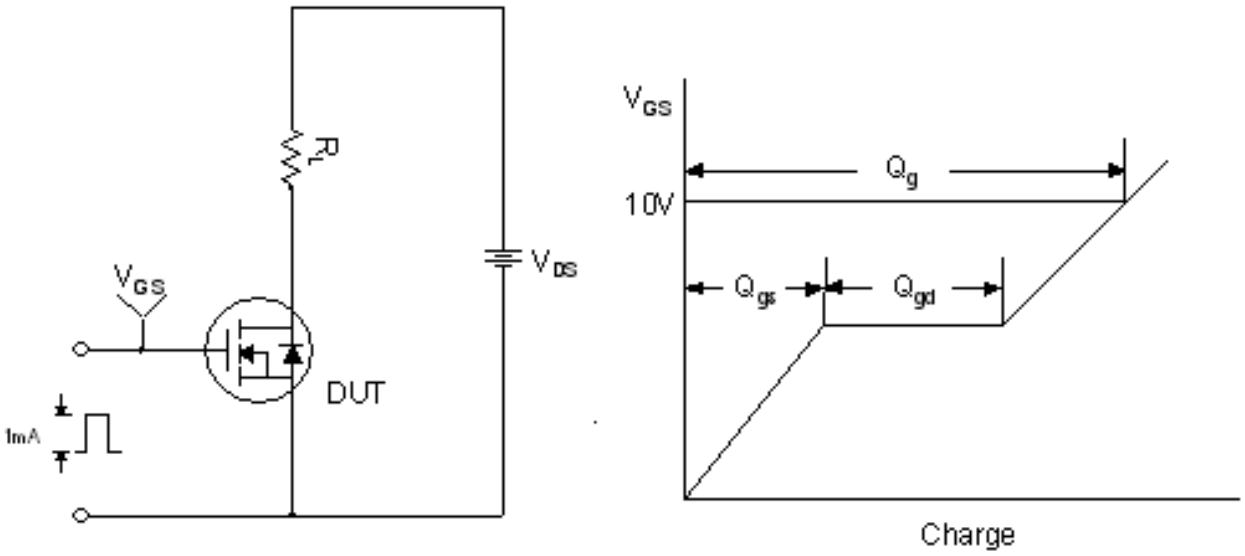


Figure 15. Gate Charge Test Circuit & Waveform

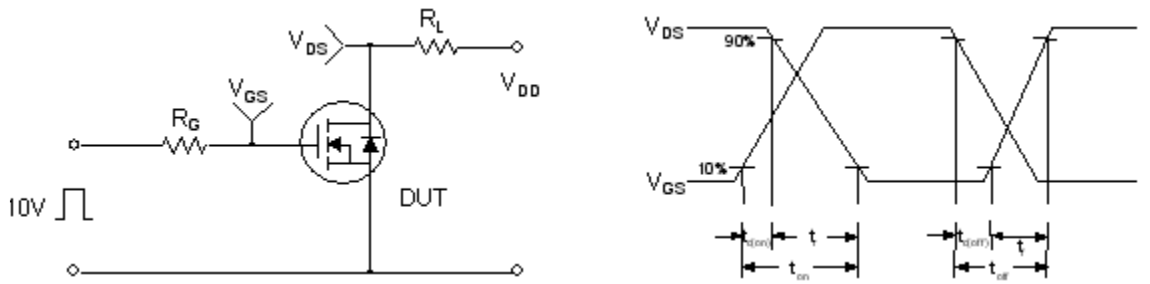


Figure 16. Resistive Switching Test Circuit & Waveforms

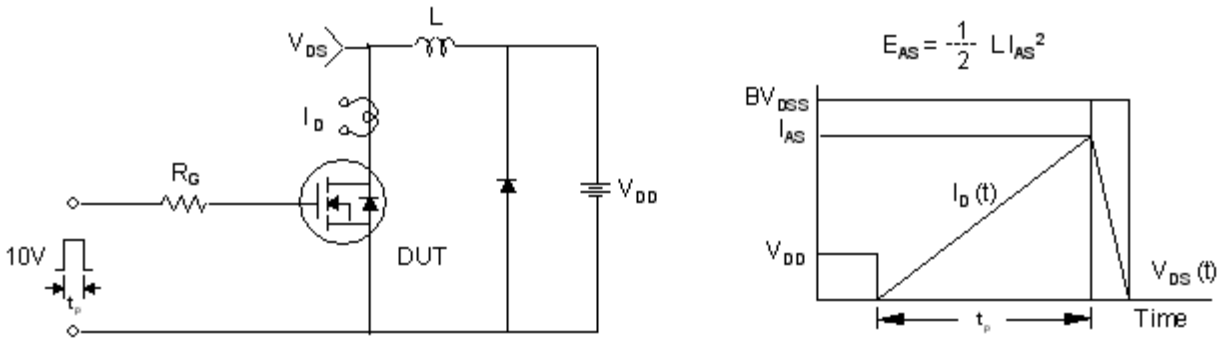


Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms

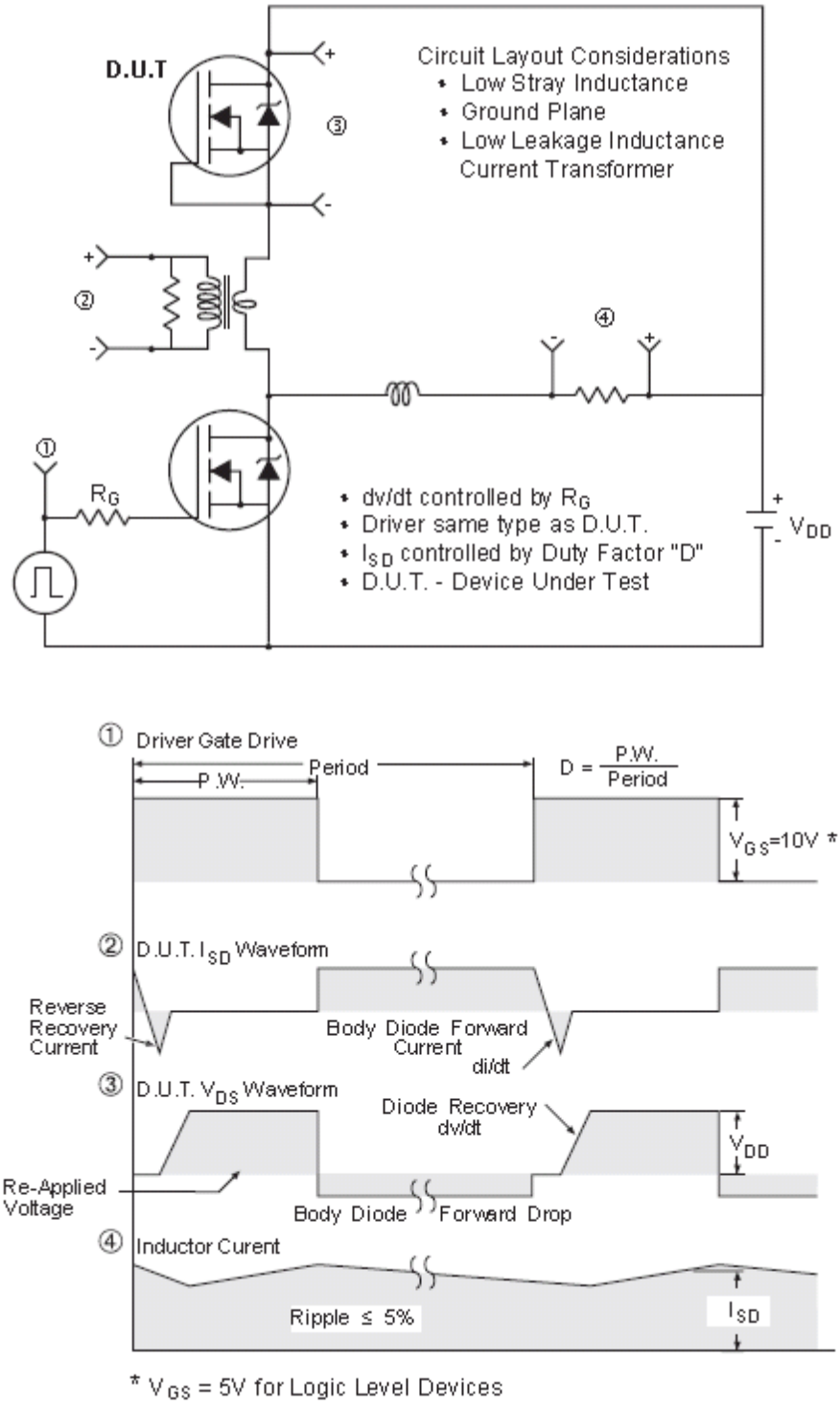
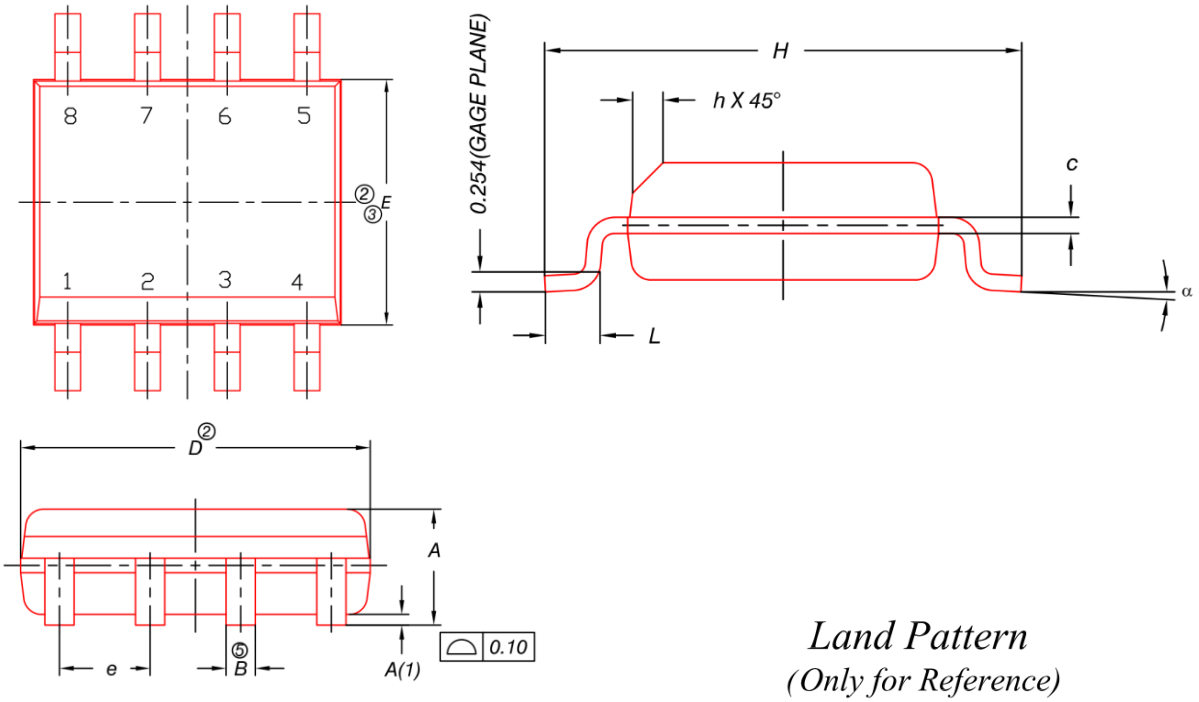
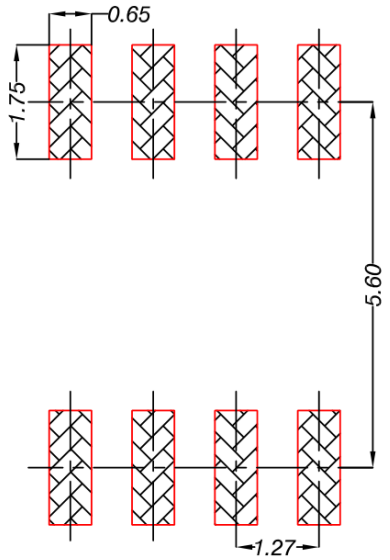


Figure 18. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

Package outline



Land Pattern
(Only for Reference)



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.35	1.55	1.75
A(1)	0.10	0.18	0.25
B	0.38	0.45	0.51
C	0.19	0.22	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
e	1.27 BSC		
H	5.80	6.00	6.20
L	0.50	0.72	0.93
α	0°	4°	8°
h	0.25	0.38	0.50

Note:
1. All Dimension Are In mm.
② Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs.
Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
③ Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
4. The Package Top May Be Smaller Than The Package Bottom.
⑤ Dimension "B" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.08 mm Total In Excess Of "B" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.

Figure 19. SOP8 Package outline

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